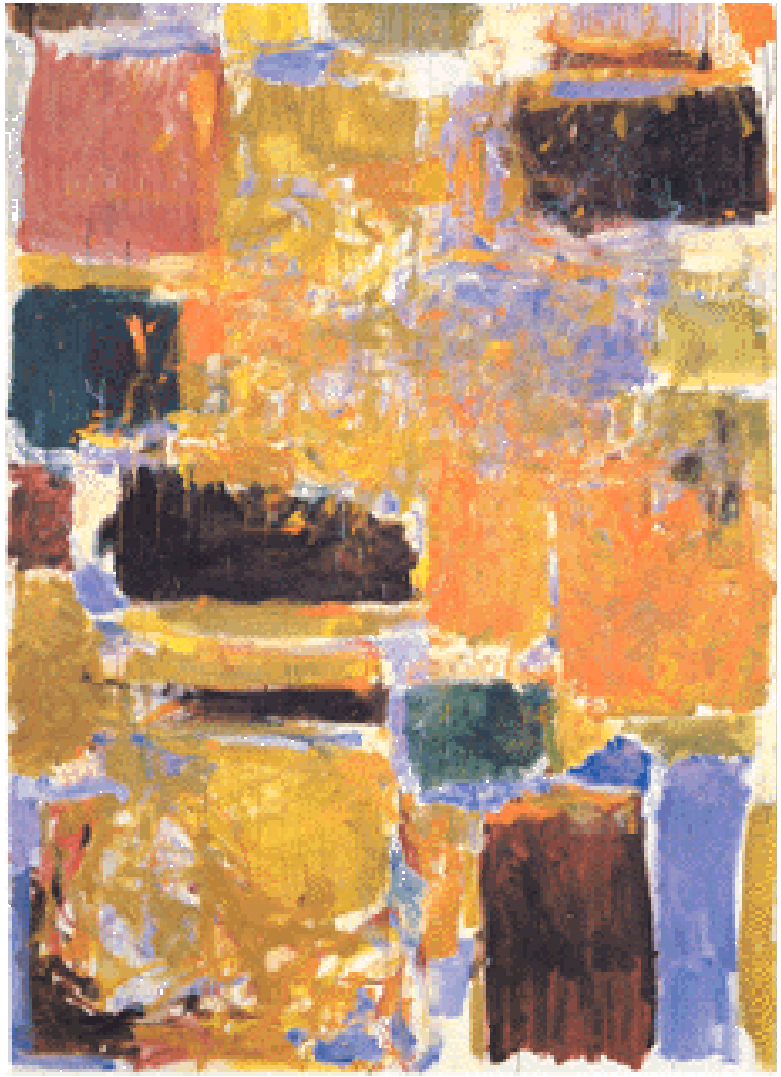
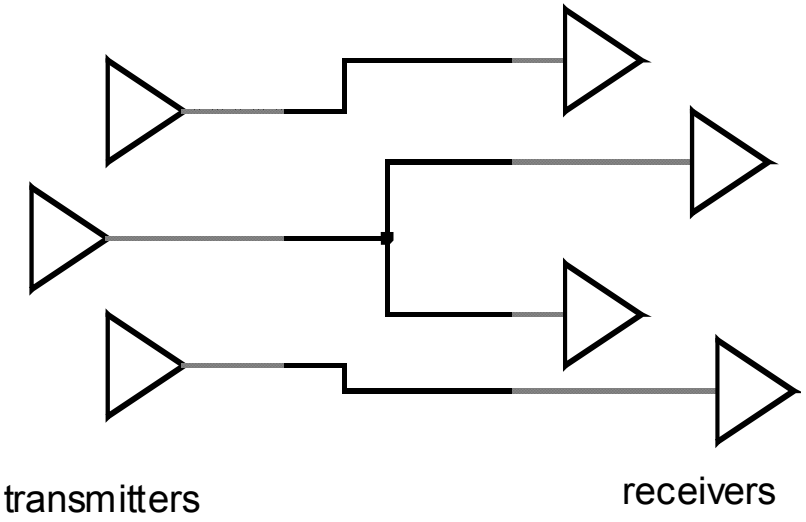


Digital Integrated Circuits

The Wire

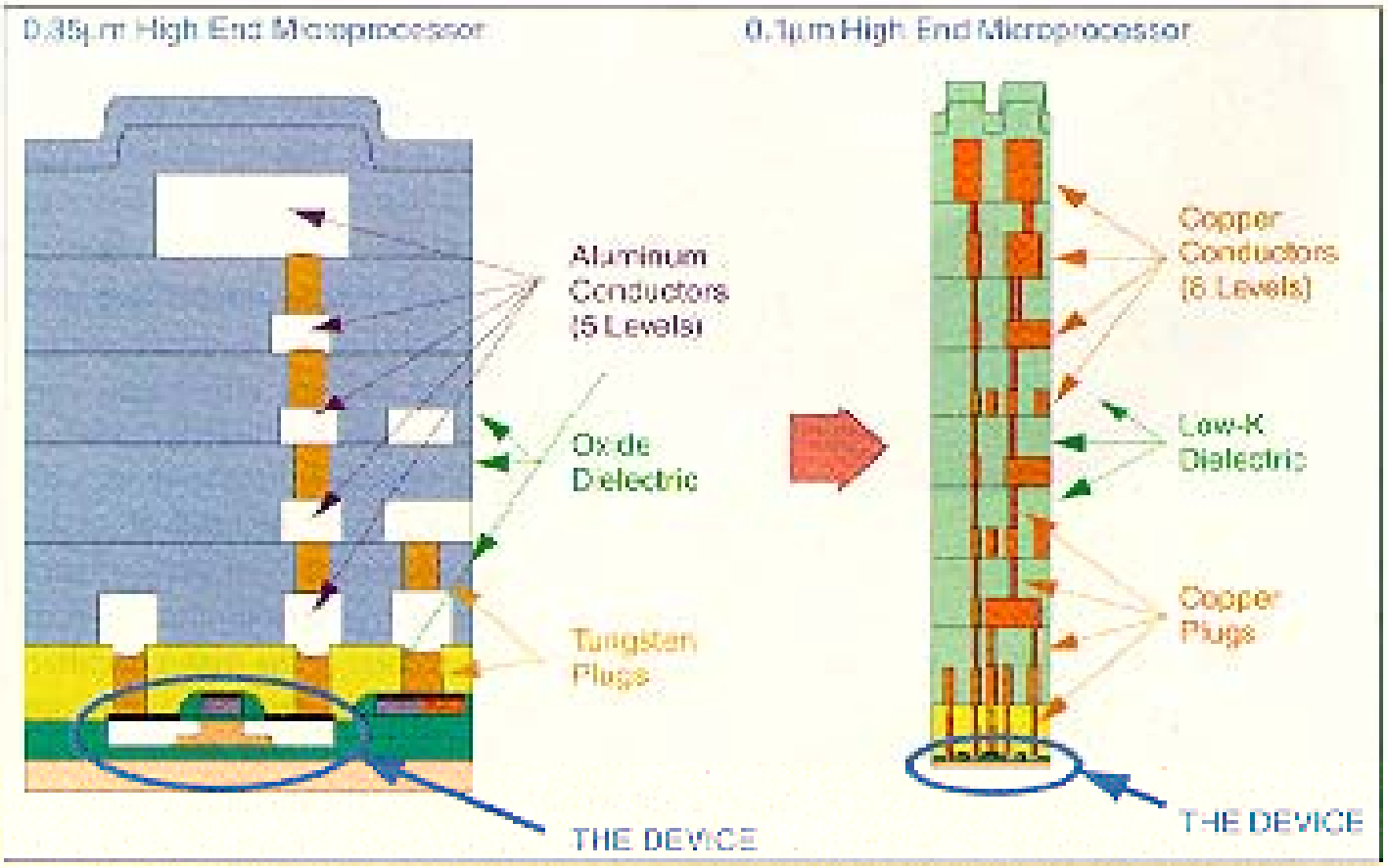
The Wire



schematics **physical**

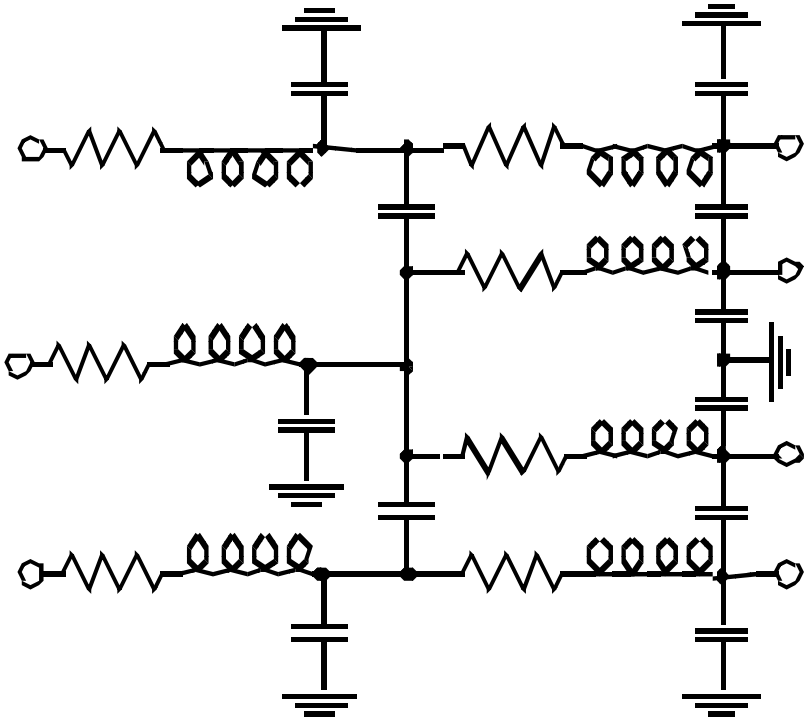
Wire?
→ metal line / poly silicon / n^+ p^+ diffusion layer → delay / power / noise (reliability)
Include all parasitic effect ?
→ Not feasible for millions of circuit nodes → circuit behavior is only determined by a few dominant parameter → clear insight into the parasitic wiring effects

Interconnect Impact on Chip

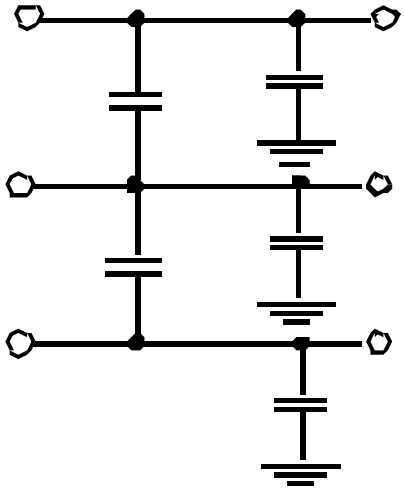


1. Process architecture challenge.

Wire Models



All-inclusive model



Capacitance-only

R, L, C

→ R , C when R ↑ or T_{rsie}/T_{fall} is slow

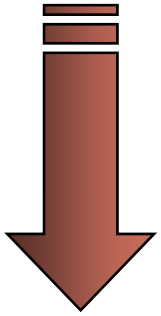
→ C only when wire is short or R ↓

→ Inter-wire C is ignored when space between wires is large

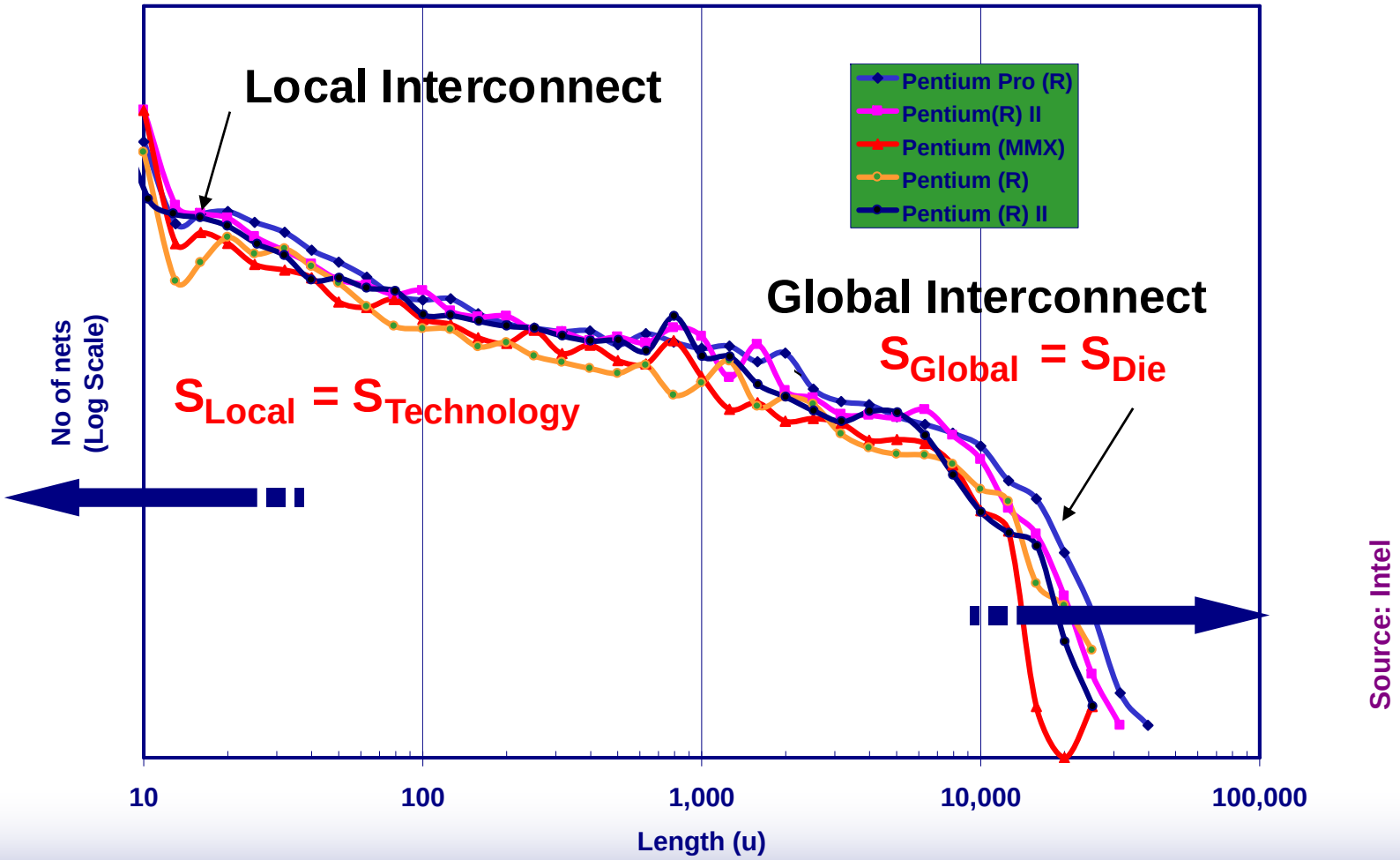
Impact of Interconnect Parasitics

- Interconnect parasitics
  - reduce reliability
  - affect performance and power consumption

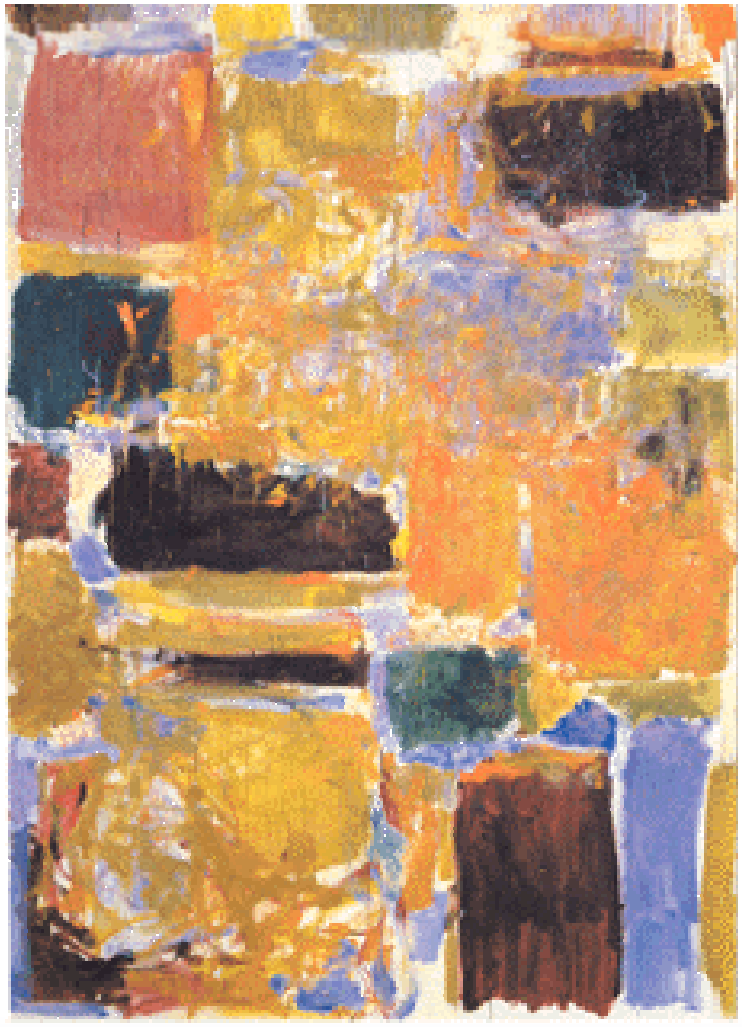
- Classes of parasitics
  - Capacitive
  - Resistive
  - Inductive



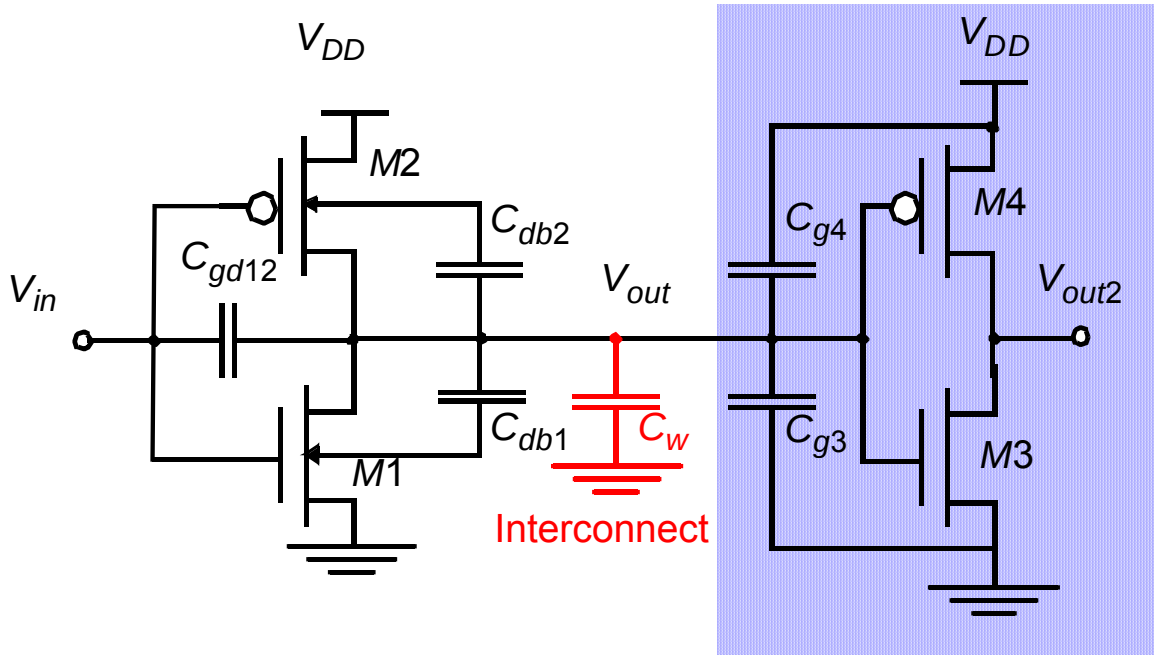
Nature of Interconnect



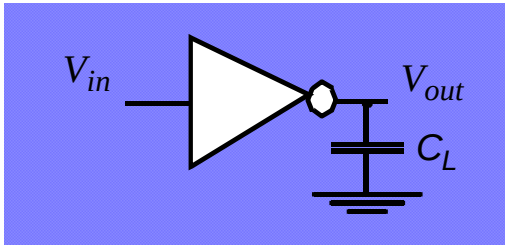
INTERCONNECT



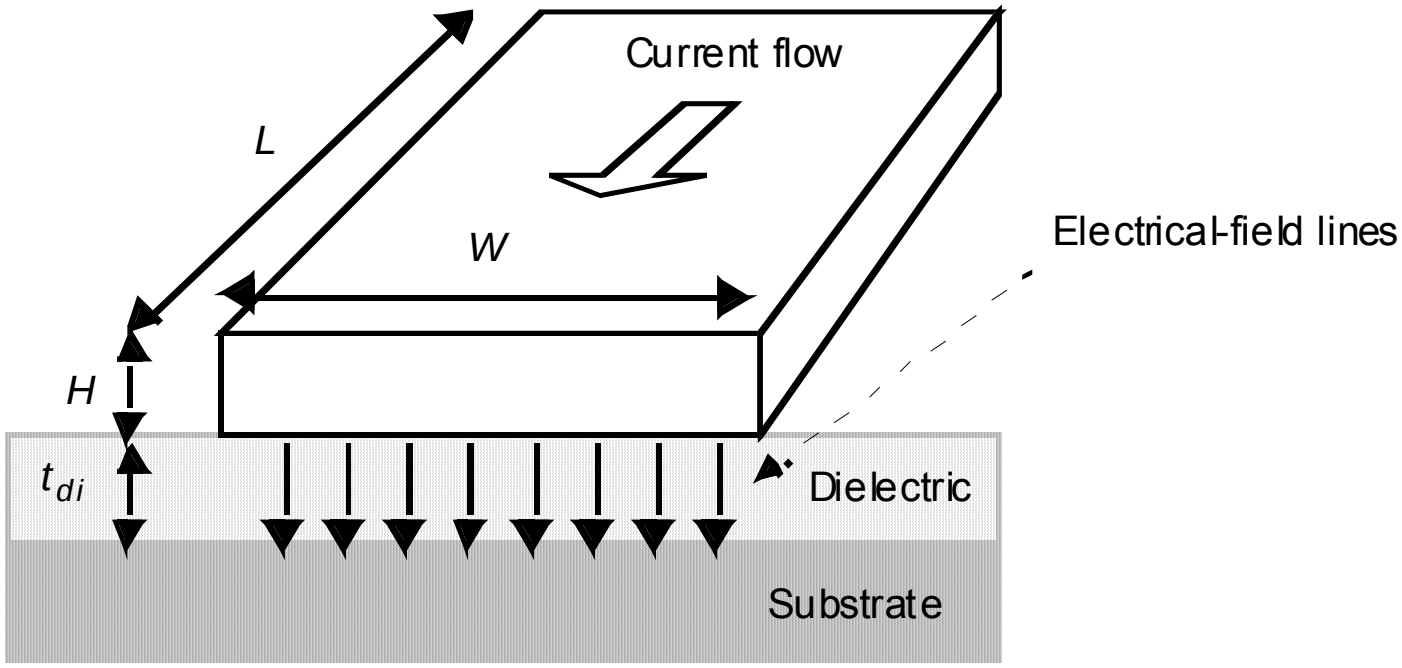
Capacitance of Wire Interconnect



Simplified Model



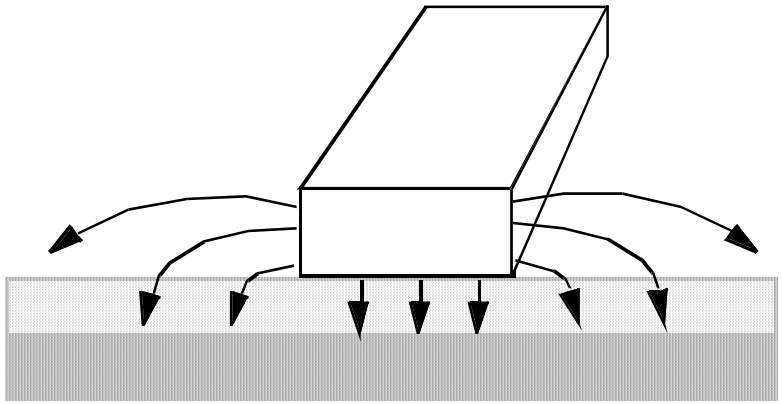
Capacitance: The Parallel Plate Model



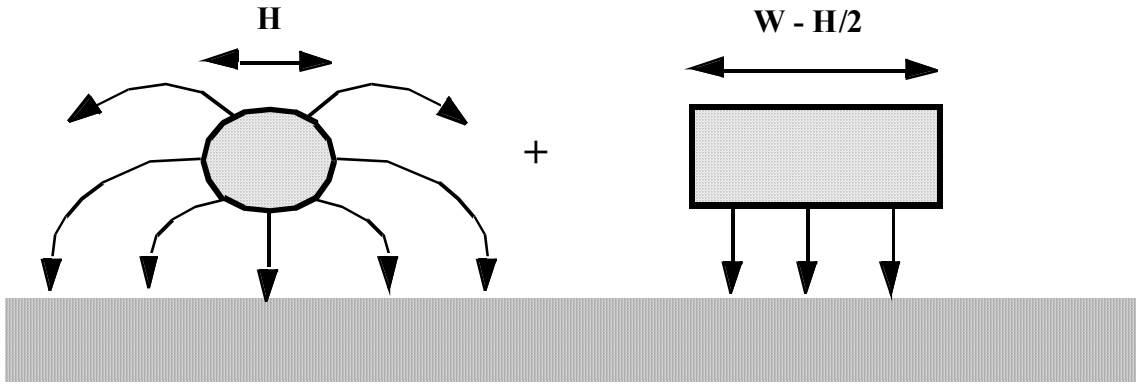
$$c_{int} = \frac{\varepsilon_{di}}{t_{di}} WL$$

$$S_{Cwire} = \frac{S}{S \cdot S_L} = \frac{1}{S_L}$$

Fringing Capacitance



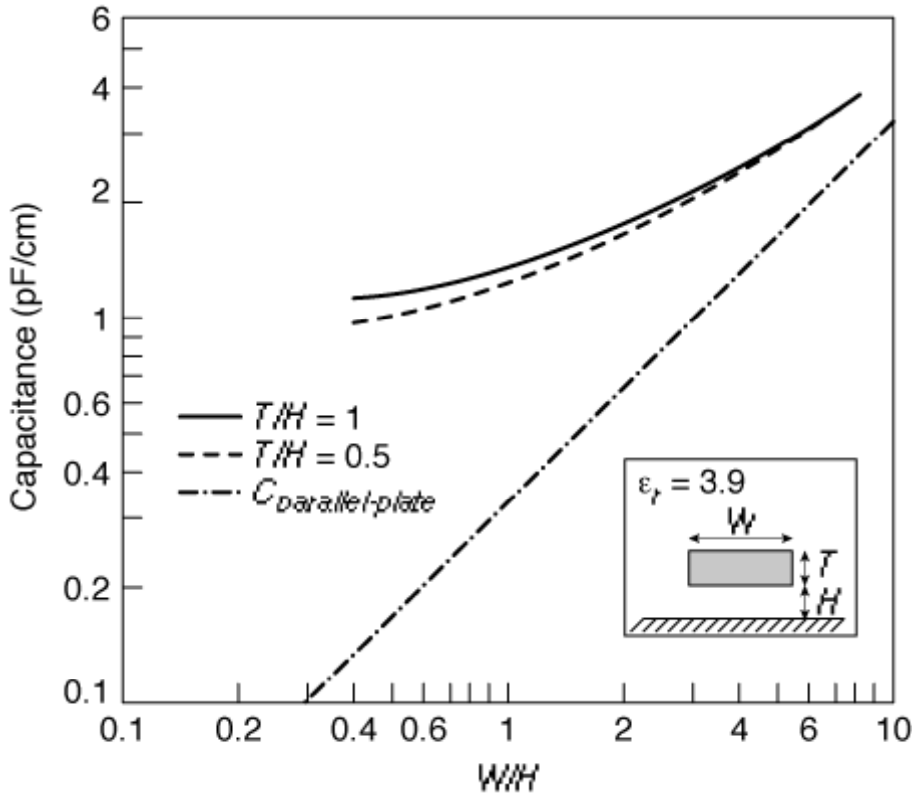
(a)



(b)

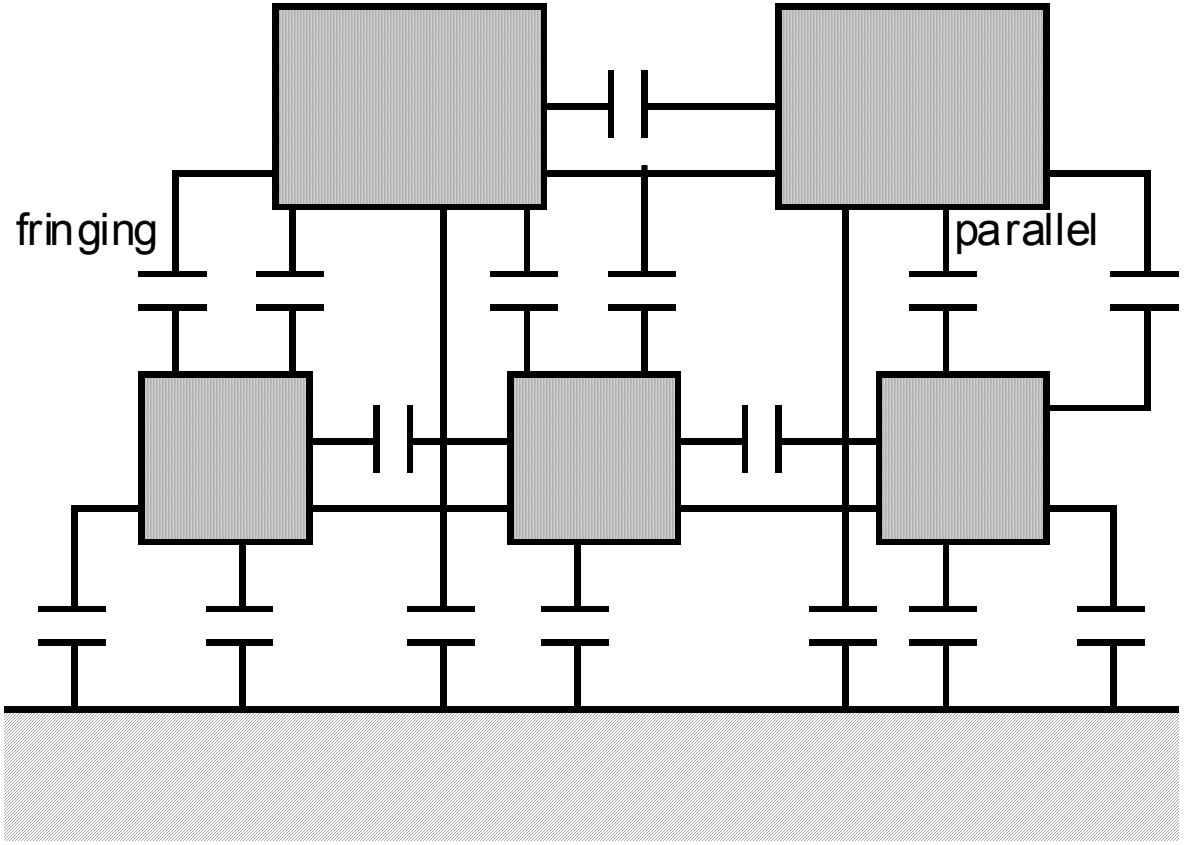
$$c_{wire} = c_{pp} + c_{fringe} = \frac{w\varepsilon_{di}}{t_{di}} + \frac{2\pi\varepsilon_{di}}{\log(t_{di}/H)}$$

Fringing versus Parallel Plate

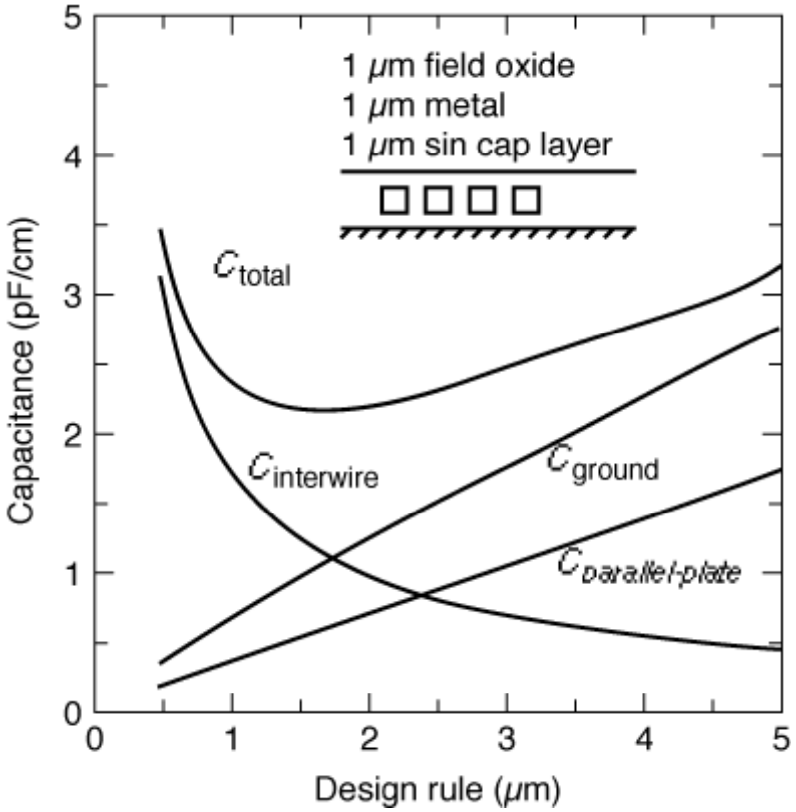


(from [Bakoglu89])

Interwire Capacitance



Impact of Interwire Capacitance



(from [Bakoglu89])

Wiring Capacitances (0.25 μm CMOS)

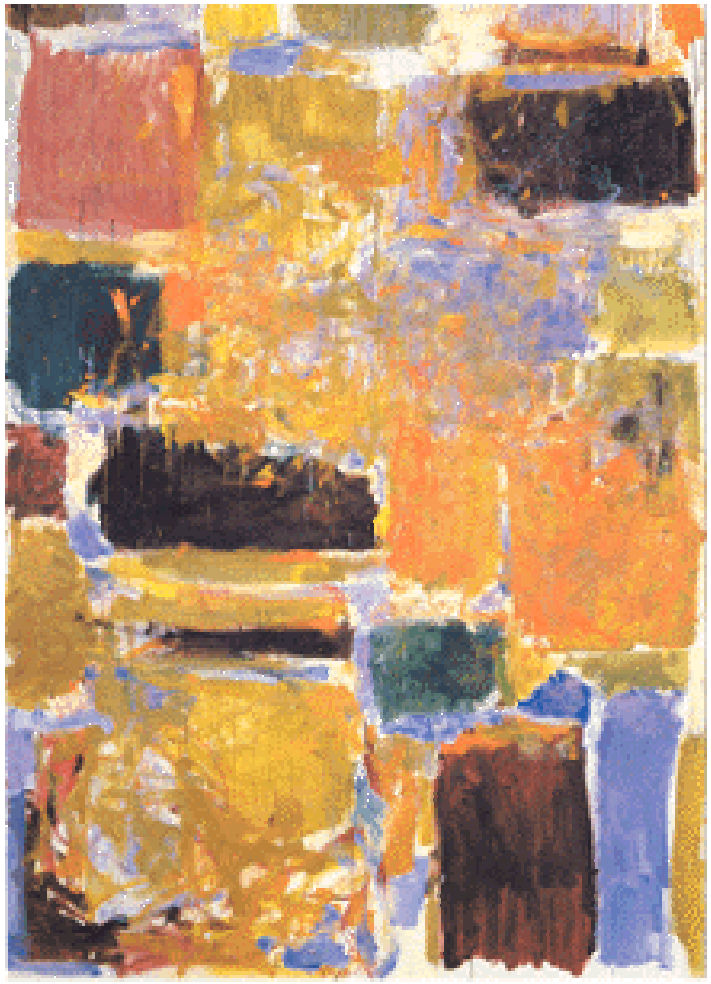
	Field	Active	Poly	Al1	Al2	Al3	Al4
Poly	88						
	54						
Al1	30	41	57				
	40	47	54				
Al2	13	15	17	36			
	25	27	29	45			
Al3	8.9	9.4	10	15	41		
	18	19	20	27	49		
Al4	6.5	6.8	7	8.9	15	35	
	14	15	15	18	27	45	
Al5	5.2	5.4	5.4	6.6	9.1	14	38
	12	12	12	14	19	27	52

Capacitance of Metal Wire

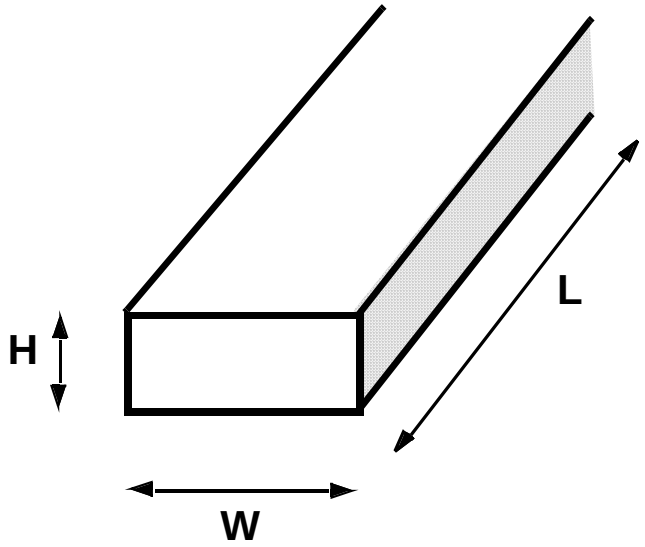
- Example
  - Al1 layer L=10cm W=1um
  - Total capacitance?

  - Total capacitance = 11pF
    - Area cap = $(0.1 \times 10^6 um^2) \times 30aF/um^2 = 3pF$
    - Fringing cap = $2 \times (0.1 \times 10^6 um^2) \times 40aF/um^2 = 8pF$

INTERCONNECT



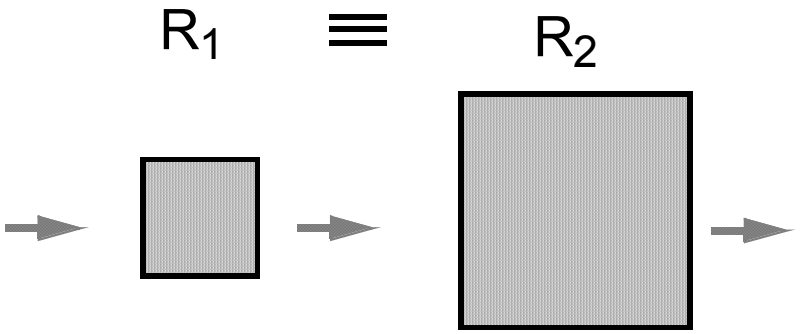
Wire Resistance



$$R = \rho \frac{L}{H\,W}$$

Sheet Resistance

R_o



Resistance of Metal Wire

- Example
  - Al1 layer L=10cm W=1um, sheet R = 0.075Ω/□
  - Polysilicon L=10cm W=1um, sheet R = 175Ω/□
  - Total Resistance ?

  - Total Resistance
    - A1 → R_{wire} = 0.075Ω/□ × (0.1×$10^6$$um^2$) / 1um =7.5KΩ
    - Polysilicon → R_{wire} = 175Ω/□ × (0.1×$10^6$$um^2$) / 1um =17.5MΩ

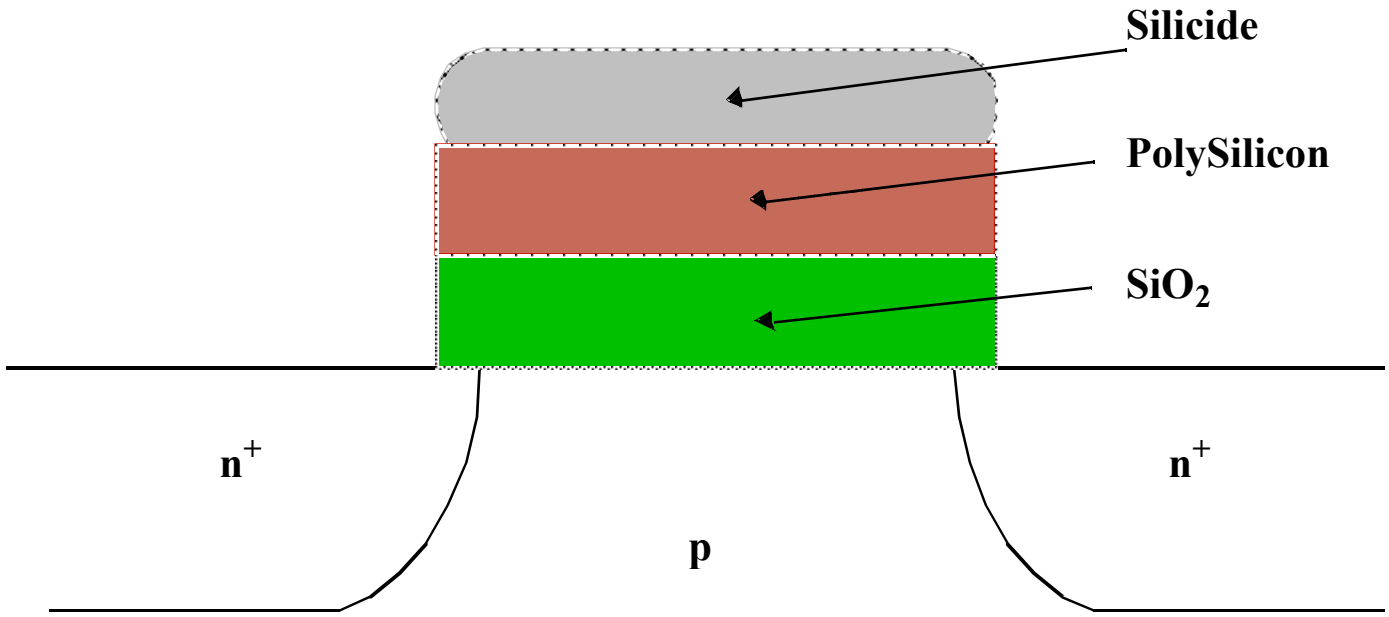
Interconnect Resistance

Material	ρ (Ω-m)
Silver (Ag)	1.6×10^{-8}
Copper (Cu)	1.7×10^{-8}
Gold (Au)	2.2×10^{-8}
Aluminum (Al)	2.7×10^{-8}
Tungsten (W)	5.5×10^{-8}

Dealing with Resistance

- **Selective Technology Scaling**
- **Use Better Interconnect Materials**
  - reduce average wire-length
  - e.g. copper, silicides
- **More Interconnect Layers**
  - reduce average wire-length

Polycide Gate MOSFET



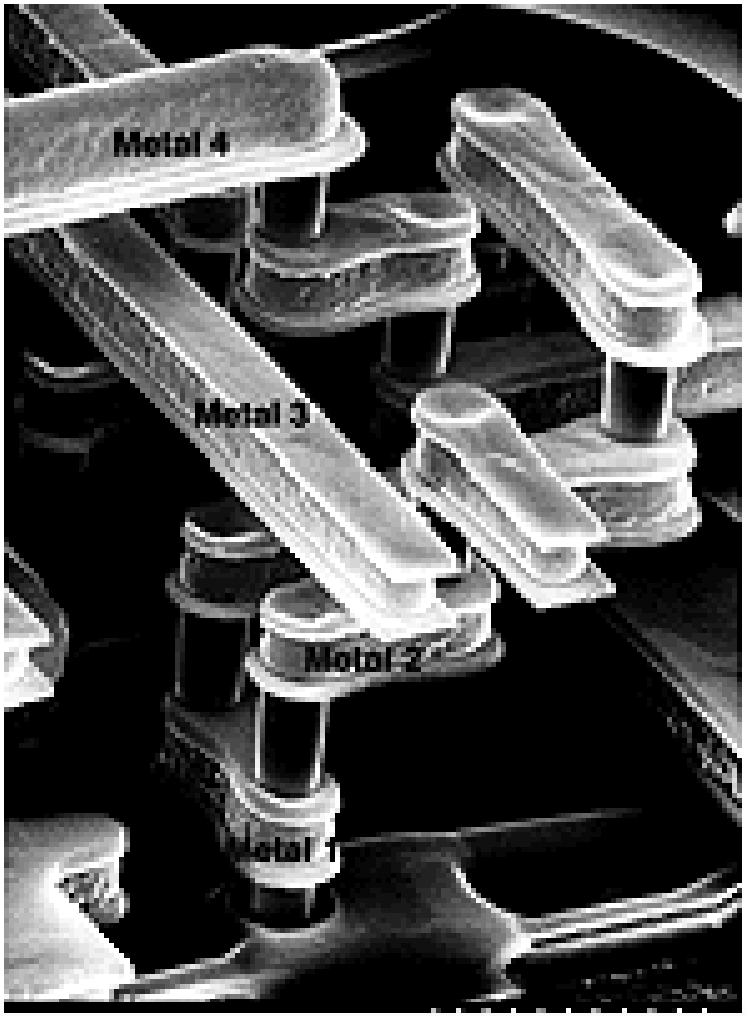
Silicides: WSi_2, $TiSi_2$, $PtSi_2$ and TaSi

Conductivity: 8-10 times better than Poly

Sheet Resistance

Material	Sheet Resistance (Ω/❑)
n- or p-well diffusion	1000 – 1500
n^+, p^+ diffusion	50 – 150
n^+, p^+ diffusion with silicide	3 – 5
n^+, p^+ polysilicon	150 – 200
n^+, p^+ polysilicon with silicide	4 – 5
Aluminum	0.05 – 0.1

Modern Interconnect

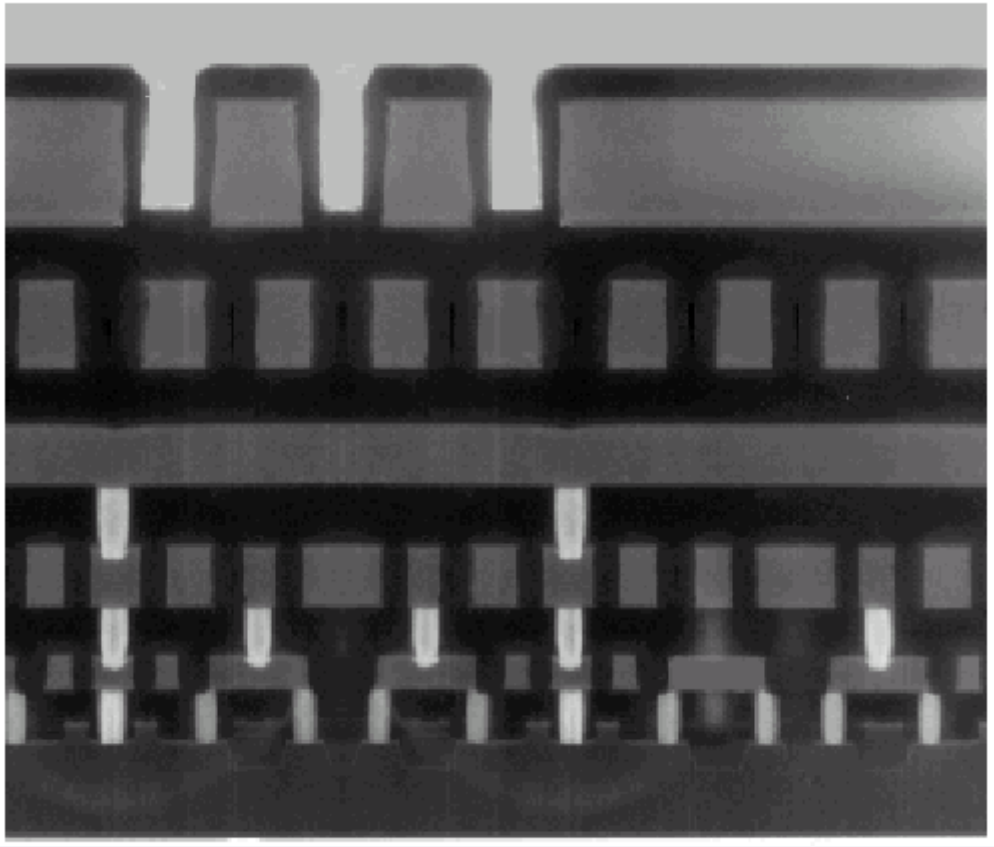


Example: Intel 0.25 micron Process

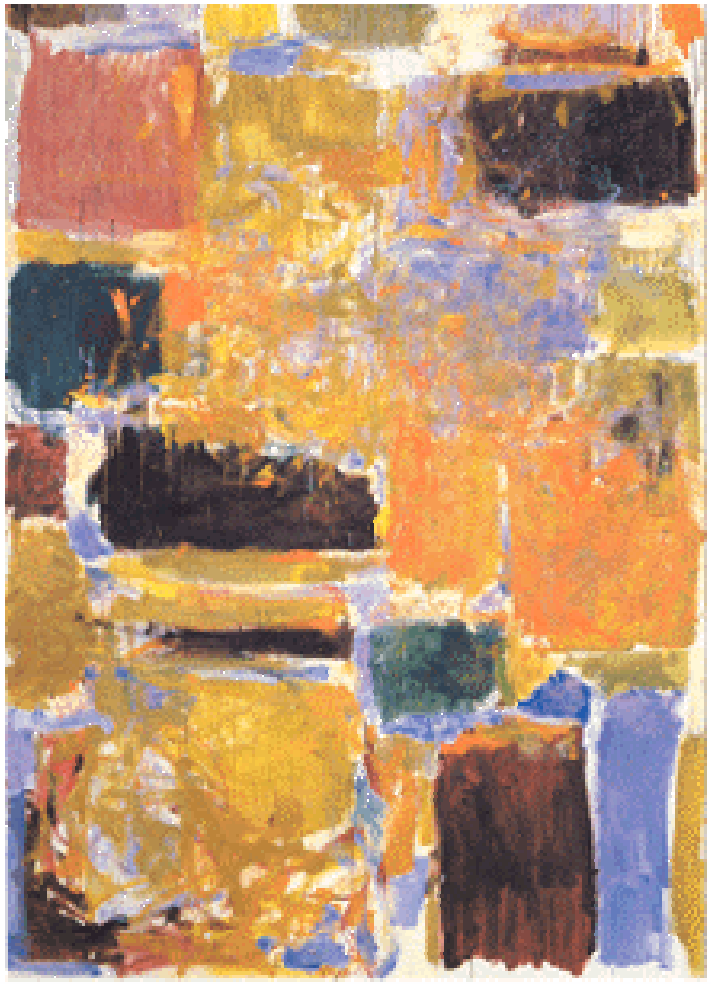
5 metal layers
Ti/Al - Cu/Ti/TiN
Polysilicon dielectric

LAYER	PITCH	THICK	A.R.
Isolation	0.67	0.40	-
Polysilicon	0.64	0.25	-
Metal 1	0.64	0.48	1.5
Metal 2	0.93	0.90	1.9
Metal 3	0.93	0.90	1.9
Metal 4	1.60	1.33	1.7
Metal 5	2.56	1.90	1.5
	µm	µm	

Layer pitch, thickness and aspect ratio



INTERCONNECT



Inductance

- ΔV = L di/dt → L?
- CL=εμ
  - ← Maxwell's law

$$v = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{\varepsilon\mu}} = \frac{C_0}{\sqrt{\varepsilon_r \mu_r}}$$

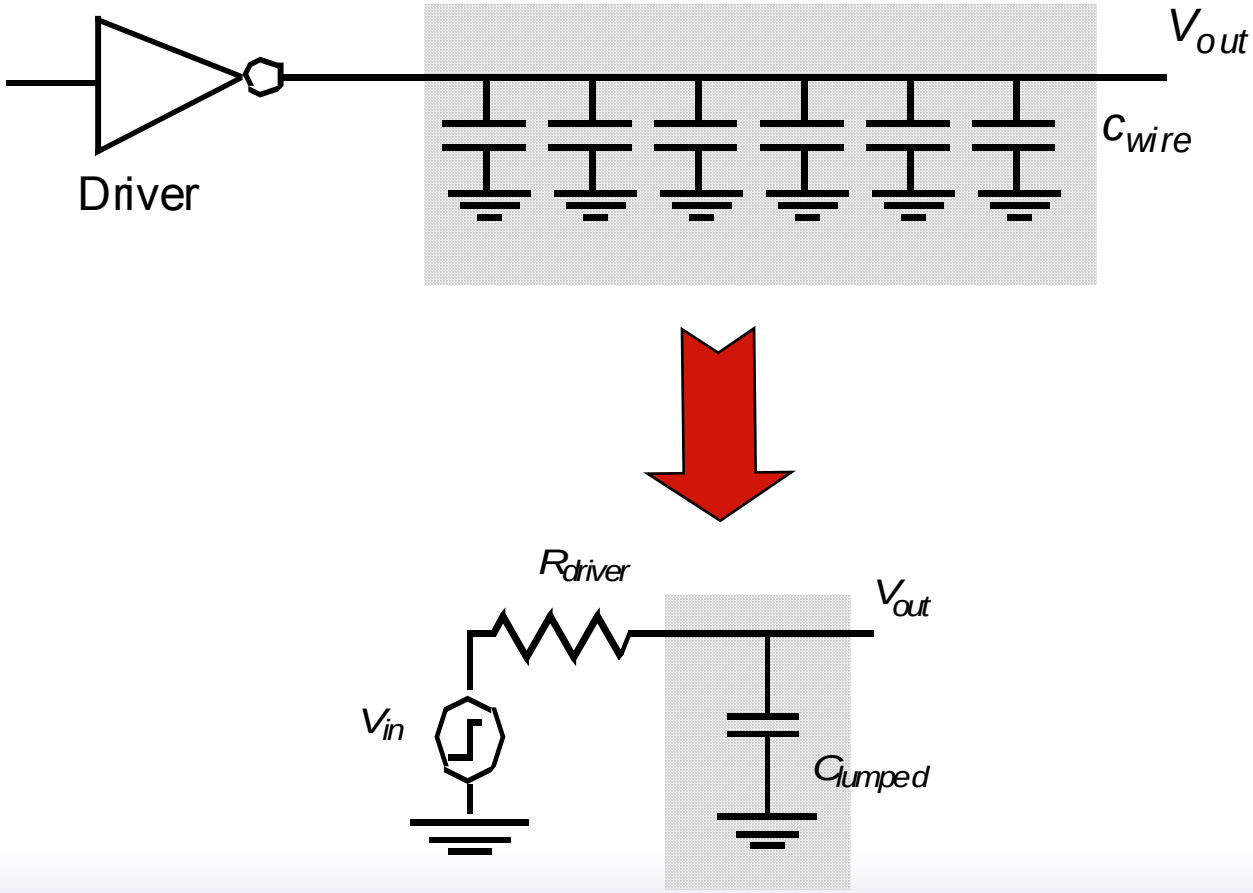
Inductance of Metal Wire

- Example
  - $C=(W\times 30+2\times 40)aF/um$
  - $L=\varepsilon\mu/C=(3.9\times 8.854\times 10^{-12})\times(4\pi\ 10^{-7})/C$
    - W=0.4um C=92aF/um L=0.47pH/um
    - W=1um C=110aF/um L=0.39pH/um
    - W=10um C=380aF/um L=0.11pH/um
  - $R=0.075/W\ \Omega/um$
  - $\omega L=R$? → 30.6GHz for W=1um

Interconnect Modeling

The Lumped Model

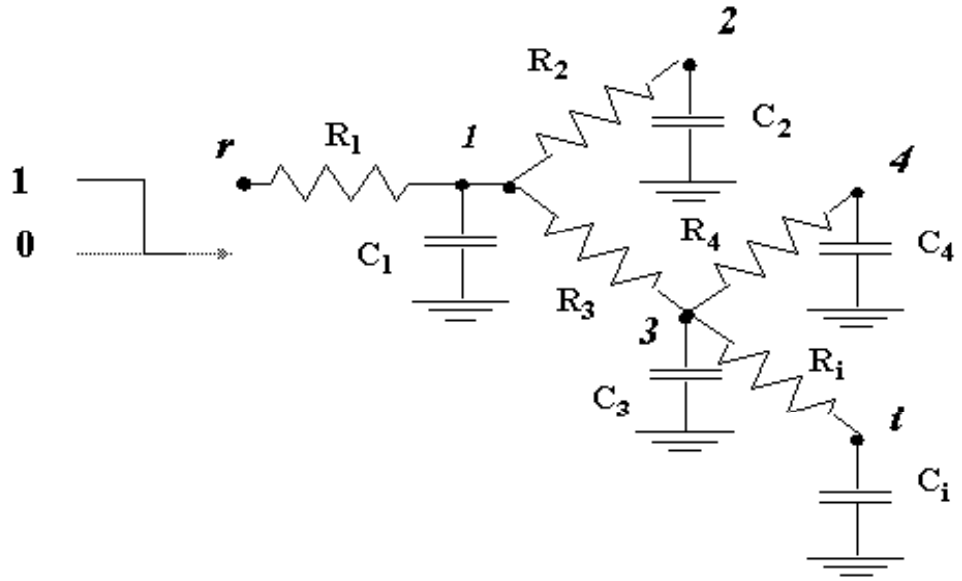
Simple but effective for digital IC



Lumped Model of Metal Wire

- Example
  - Al1 layer L=10cm W=1um → C_{lumped} = 11pF
  - R_{driver} = 10KΩ
  - $Vout(t) = (1-e^{-t/\tau})V$
    - $\tau = R_{driver} \times C_{lumped} = 10K\Omega \times 11pF$
    - 50% → $t = \ln(2)\,\tau = 0.69\,\tau = 76ns$
    - 90% → $t = \ln(9)\,\tau = 2.2\,\tau = 242ns$

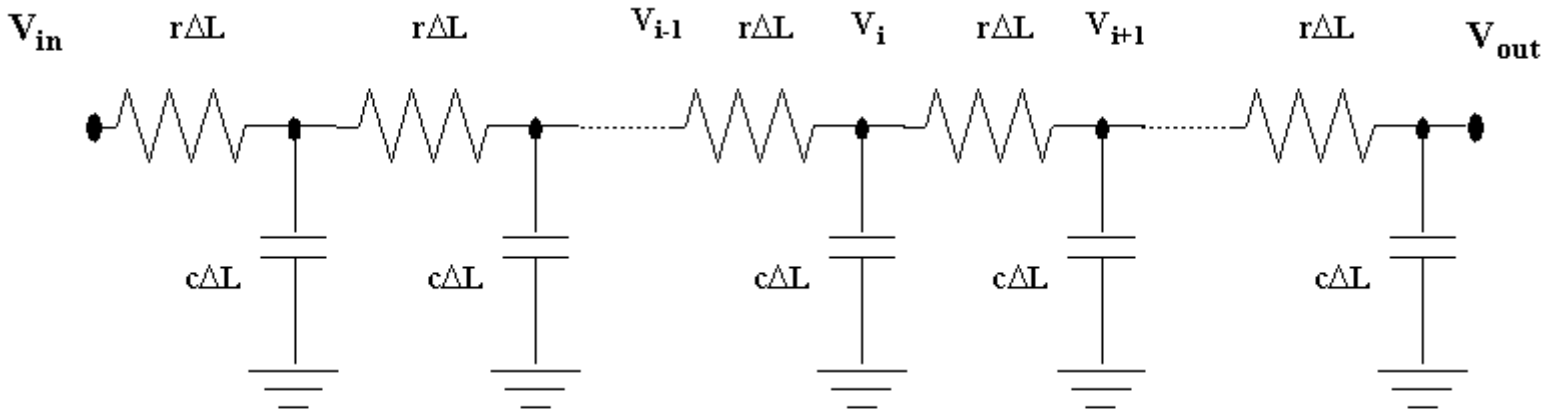
Lumped RC-Model (Elmore Delay)



$$R_{ik} = \sum_{N} R_j \Rightarrow (R_j \in [path(s \rightarrow i) \cap path(s \rightarrow k)])$$

$$\tau_{Di} = \sum_{k=1} C_k R_{ik}$$

The Elmore Delay - RC Chain



$$\tau_N = \sum_{i=1}^{N} R_i \sum_{j=i}^{N} C_j = \sum_{i=1}^{N} C_i \sum_{j=1}^{i} R_j$$

Wire Model

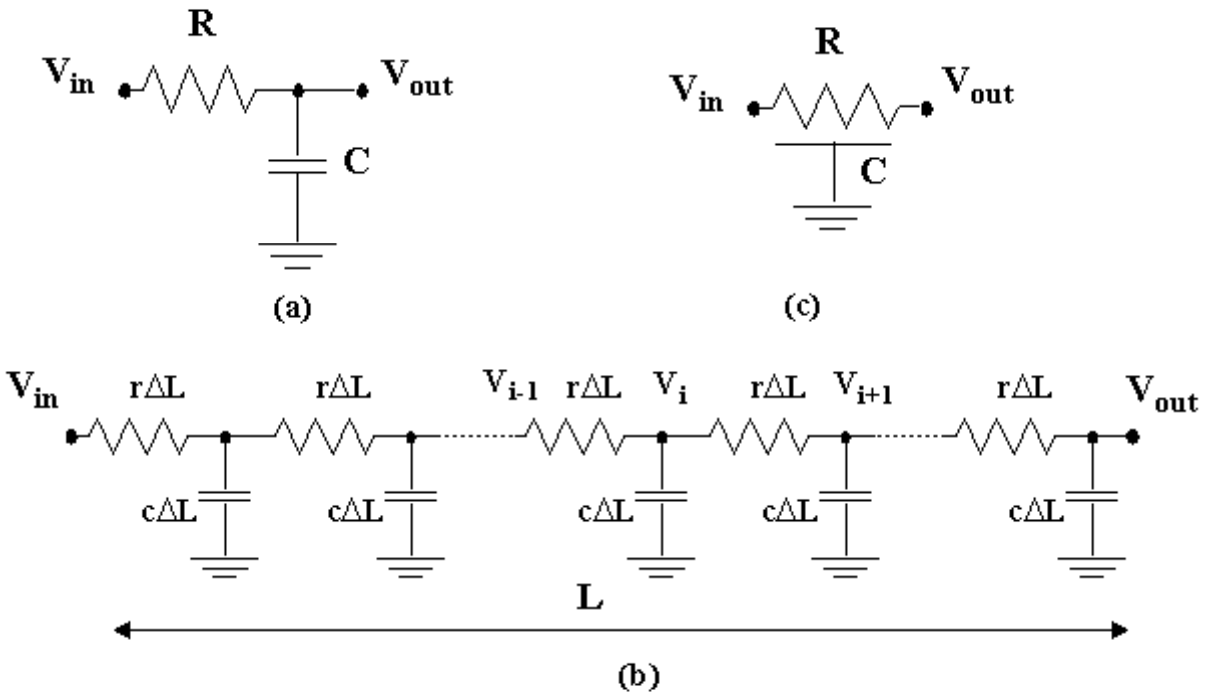
Assume: Wire modeled by N equal-length segments

$$\tau_{DN} = \left(\frac{L}{N}\right)^2 (rc + 2rc + \ldots + Nrc) = (rcL^2)\frac{N(N+1)}{2N^2} = RC\frac{N+1}{2N}$$

For large values of N:

$$\tau_{DN} = \frac{RC}{2} = \frac{rcL^2}{2}$$

The Distributed RC-line

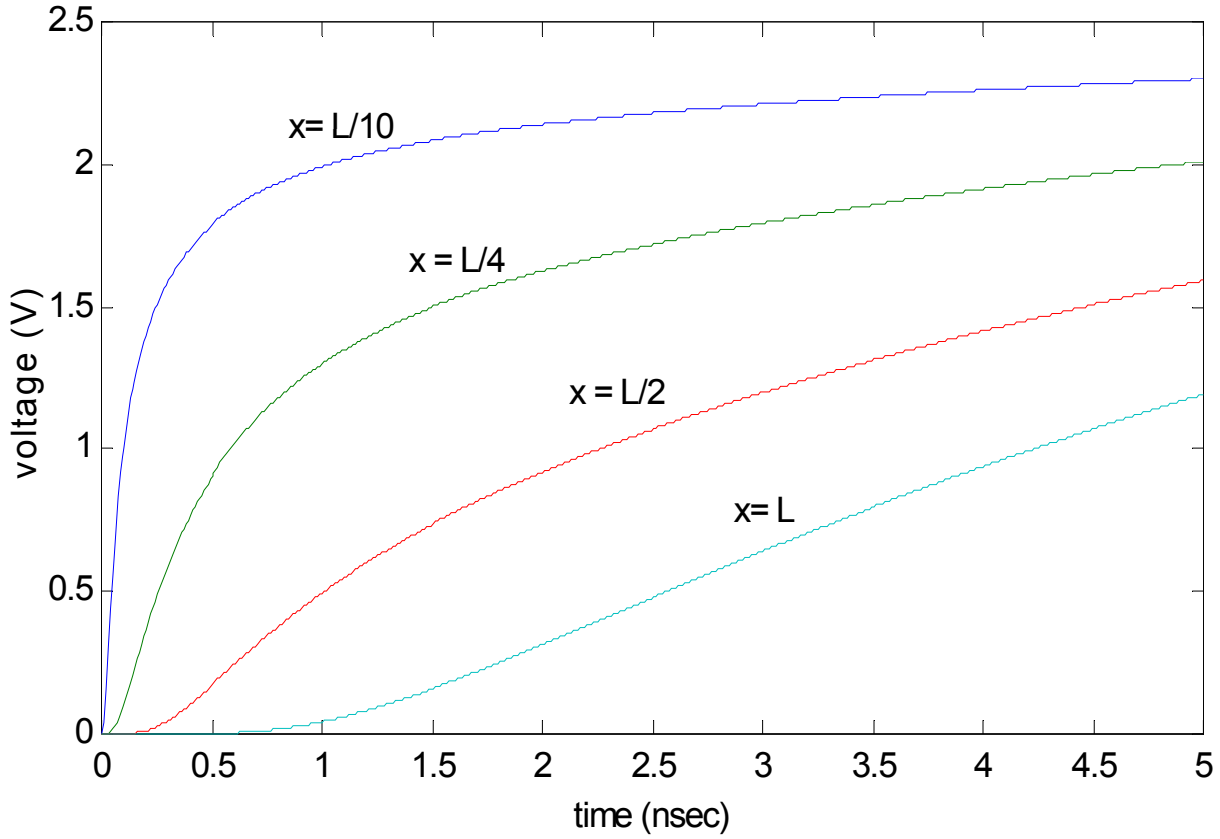


$$rc\frac{\partial V}{\partial t} = \frac{\partial^2 V}{\partial x^2}$$

The diffusion equation

$$\tau(V_{out}) = \frac{rc\,L^2}{2}$$

Step-response of RC wire as a function of time and space

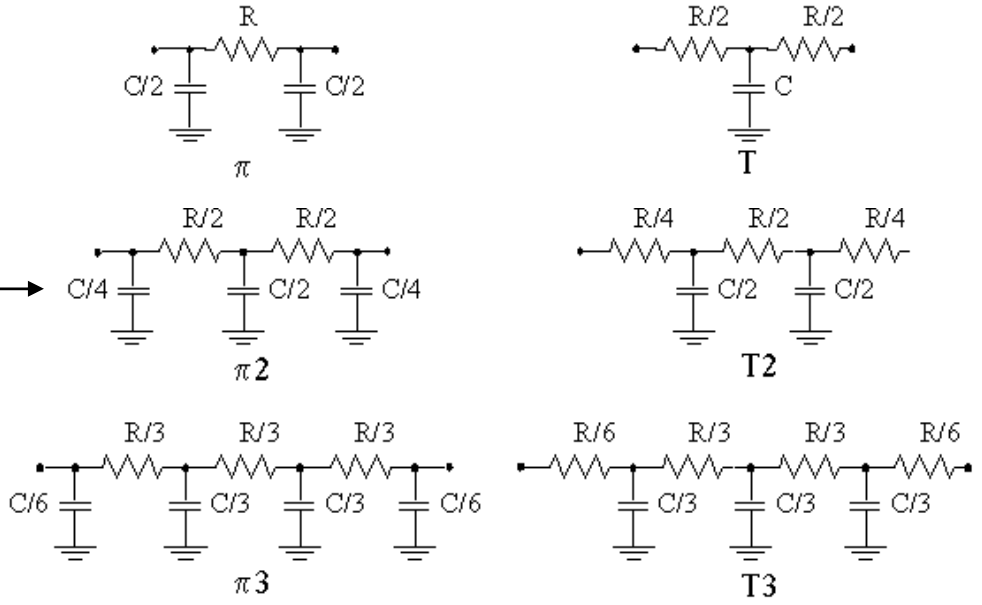


RC-Models

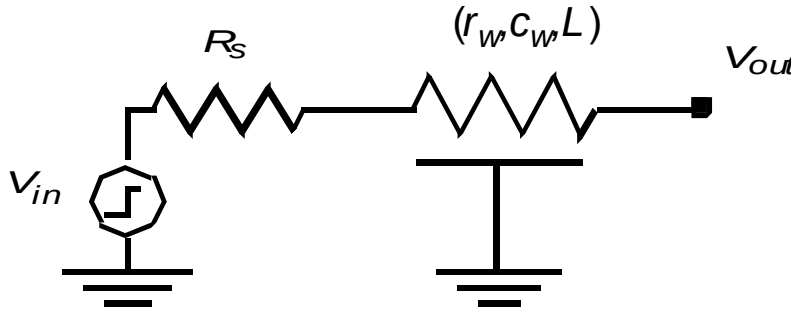
Voltage Range	Lumped RC-network	Distributed RC-network
0→50% (t_p)	0.69 RC	0.38 RC
0→63% (τ)	RC	0.5 RC
10%→90% (t_r)	2.2 RC	0.9 RC

Step Response of Lumped and Distributed RC Networks: Points of Interest.

π model → error = less 3%



Driving an RC-line



$$\tau_D = R_s C_w + \frac{R_w C_w}{2} = R_s C_w + 0.5 r_w c_w L^2$$

$$t_p = 0.69 R_s C_w + 0.38 R_w C_w$$

Design Rules of Thumb

- rc delays should only be considered when t_{pRC} >> t_{pgate} of the driving gate

$$\text{Lcrit} >> \sqrt{t_{pgate}/0.38rc}$$

- rc delays should only be considered when the rise (fall) time at the line input is smaller than RC, the rise (fall) time of the line

$$t_{rise} < RC$$

  - when not met, the change in the signal is slower than the propagation delay of the wire