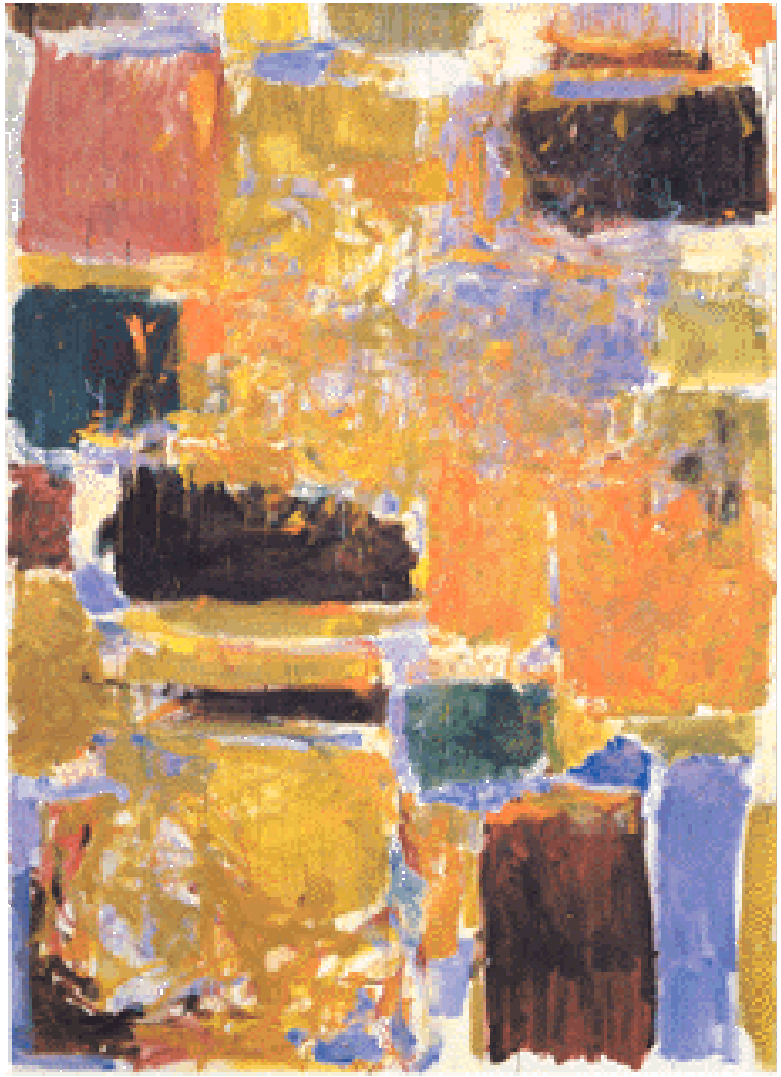


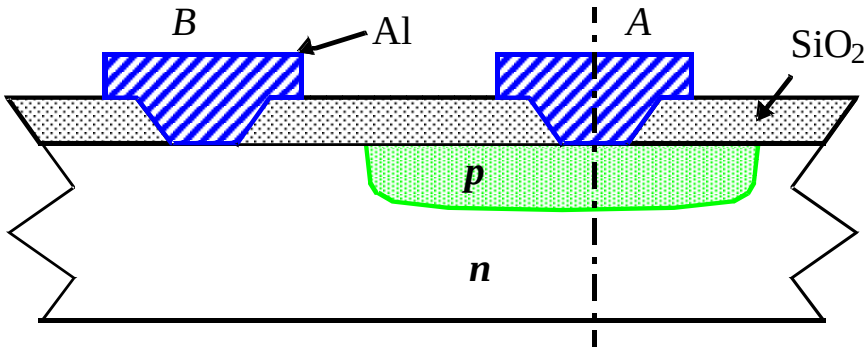
Digital Integrated Circuits

The Devices

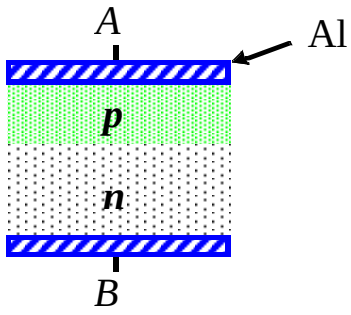
Goal of this chapter

- Present intuitive understanding of device operation
- Introduction of basic device equations
- Introduction of models for manual analysis
- Introduction of models for SPICE simulation
- Analysis of secondary and deep-sub-micron effects
- Future trends

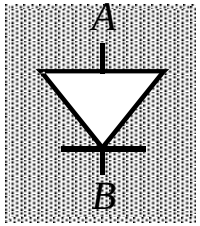
The Diode



Cross-section of *pn*-junction in an IC process



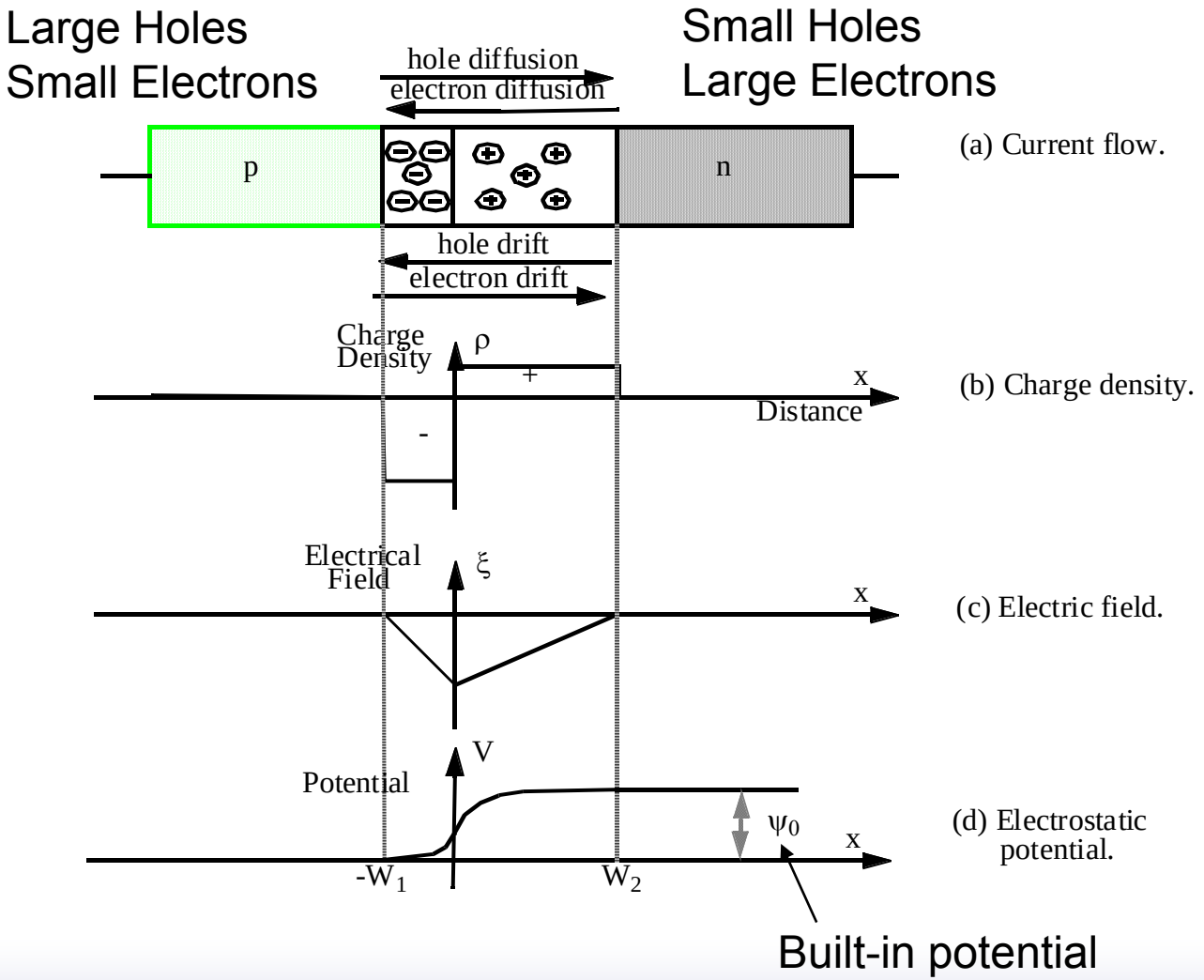
One-dimensional representation



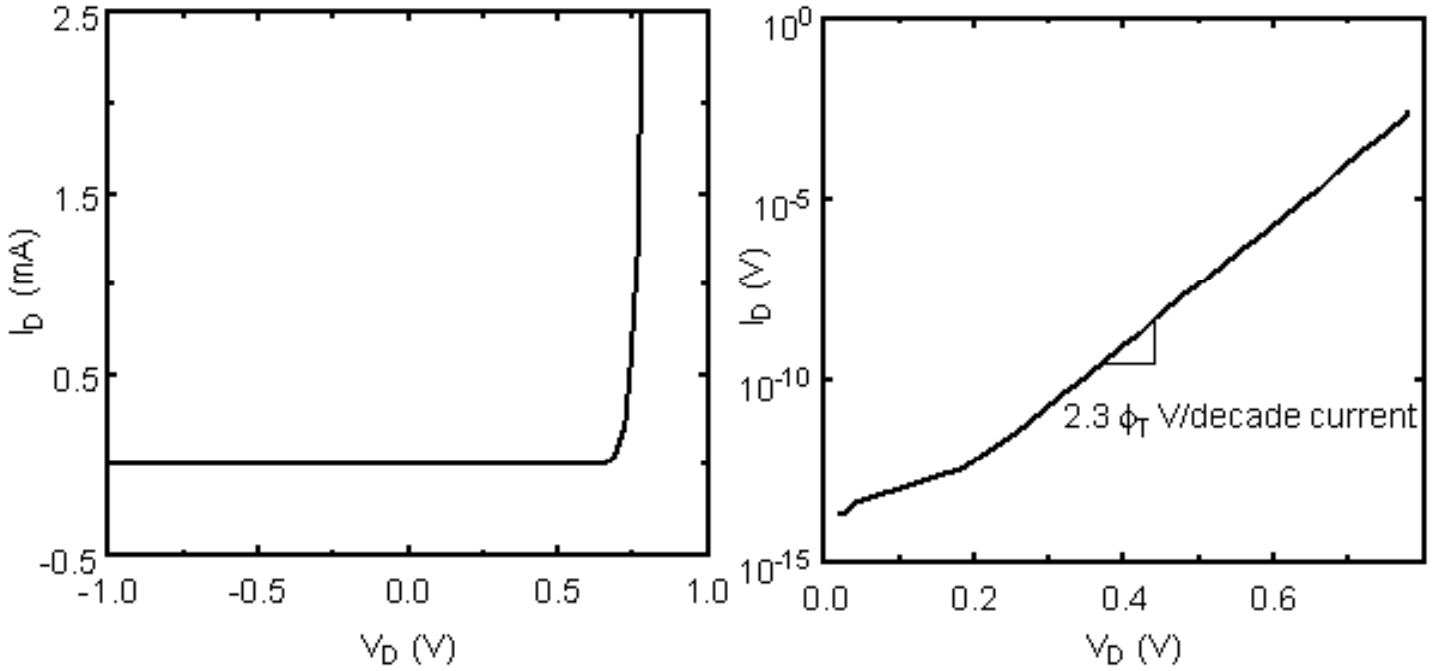
diode symbol

Mostly occurring as parasitic element in Digital ICs

Depletion Region



Diode Current

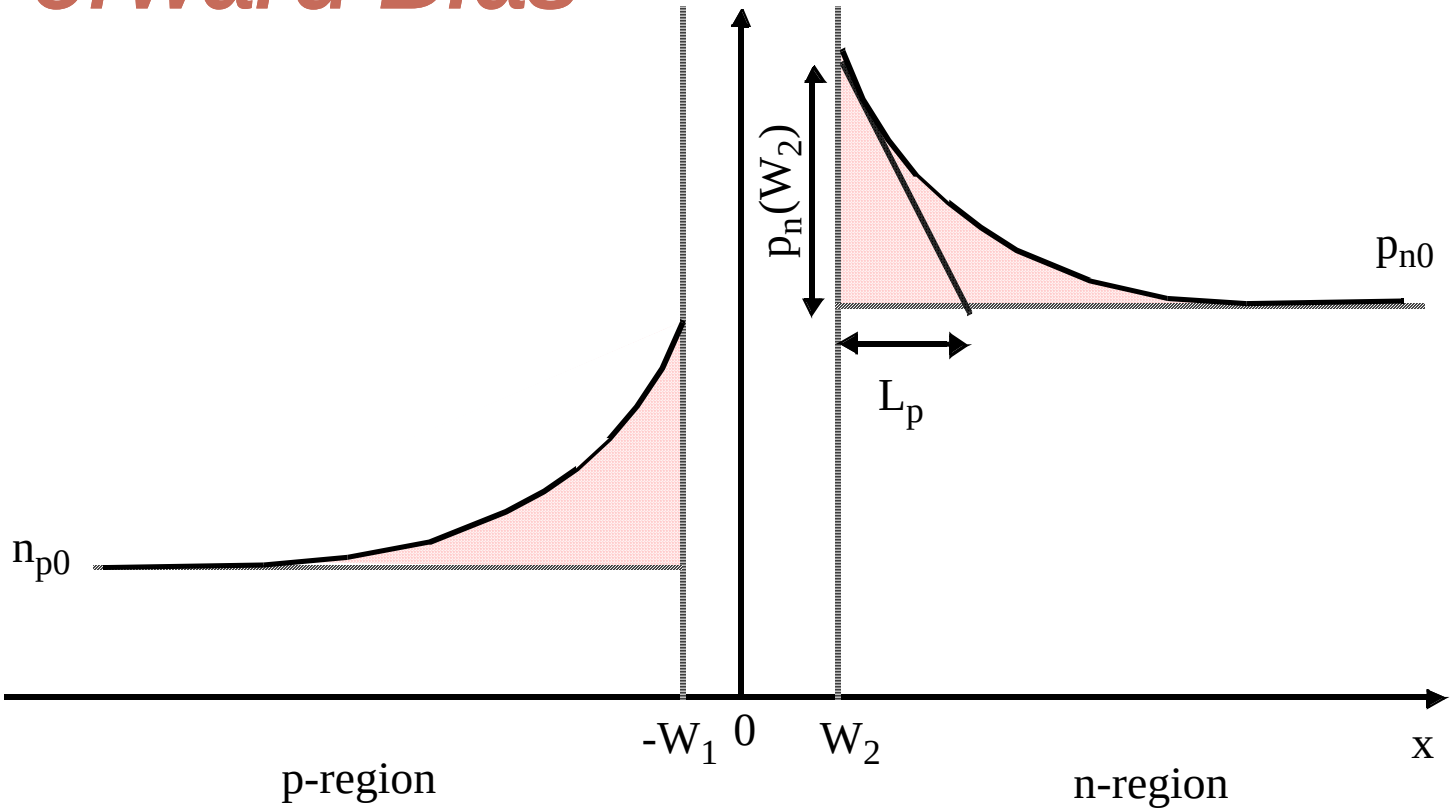


(a) On a linear scale.

(b) On a logarithmic scale (forward bias).

$$I_D = I_S\left(e^{V_D/\phi_T} - 1\right)$$

Forward Bias

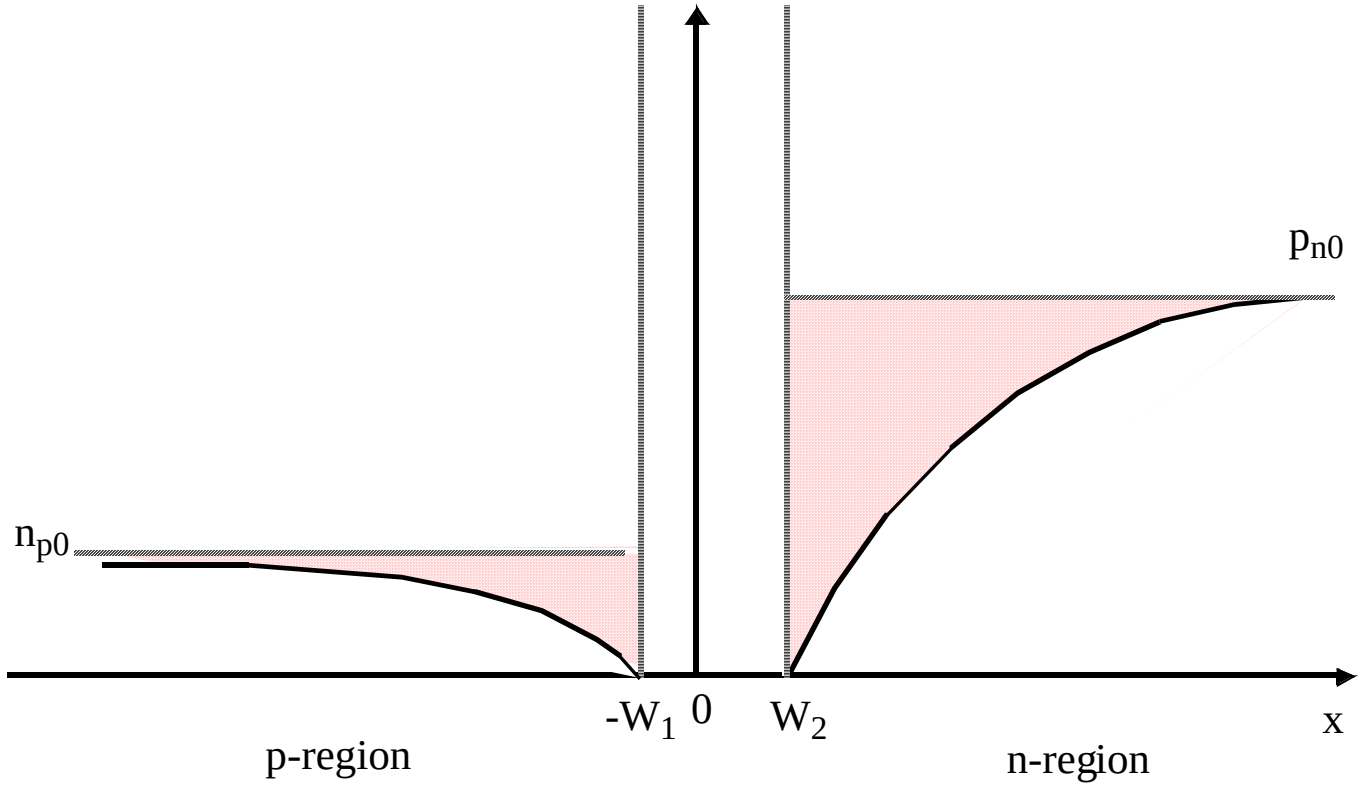


Forward voltage lowers the potential barrier
→ diffusion currents increase

diffusion

Typically avoided in Digital ICs

Reverse Bias

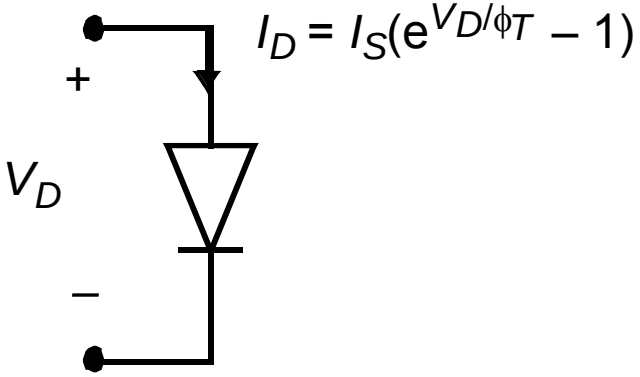


Reverse voltage raises the potential barrier
→ diffusion currents reduce

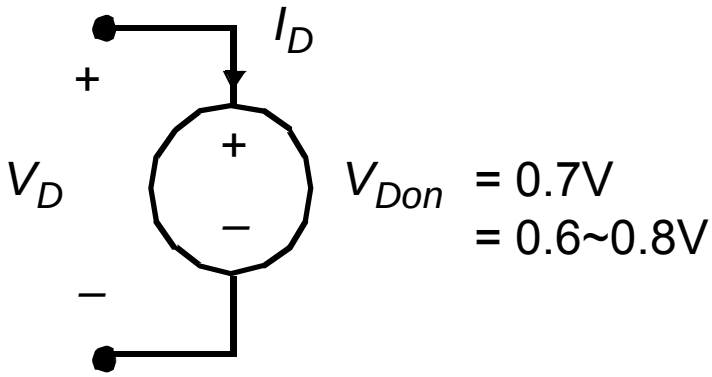
diffusion

The Dominant Operation Mode

Models for Manual Analysis



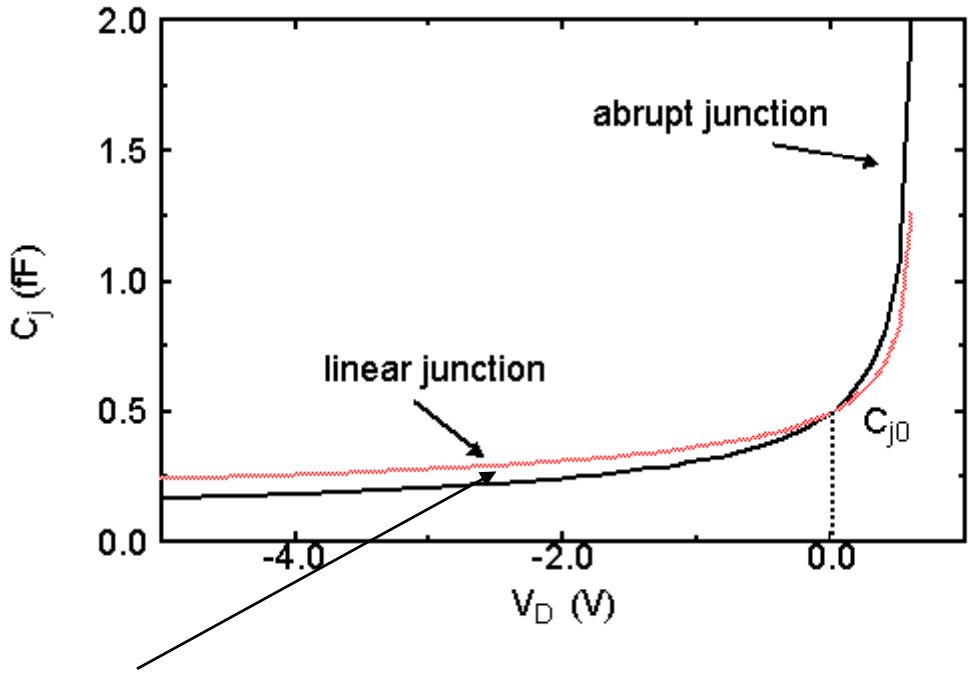
(a) Ideal diode model



(b) First-order diode model

Junction Capacitance

Forward bias ↑→ potential barrier ↓ → depletion region ↓→ cap. ↑
Reverse bias ↑→ potential barrier ↑ → depletion region ↑→ cap. ↓

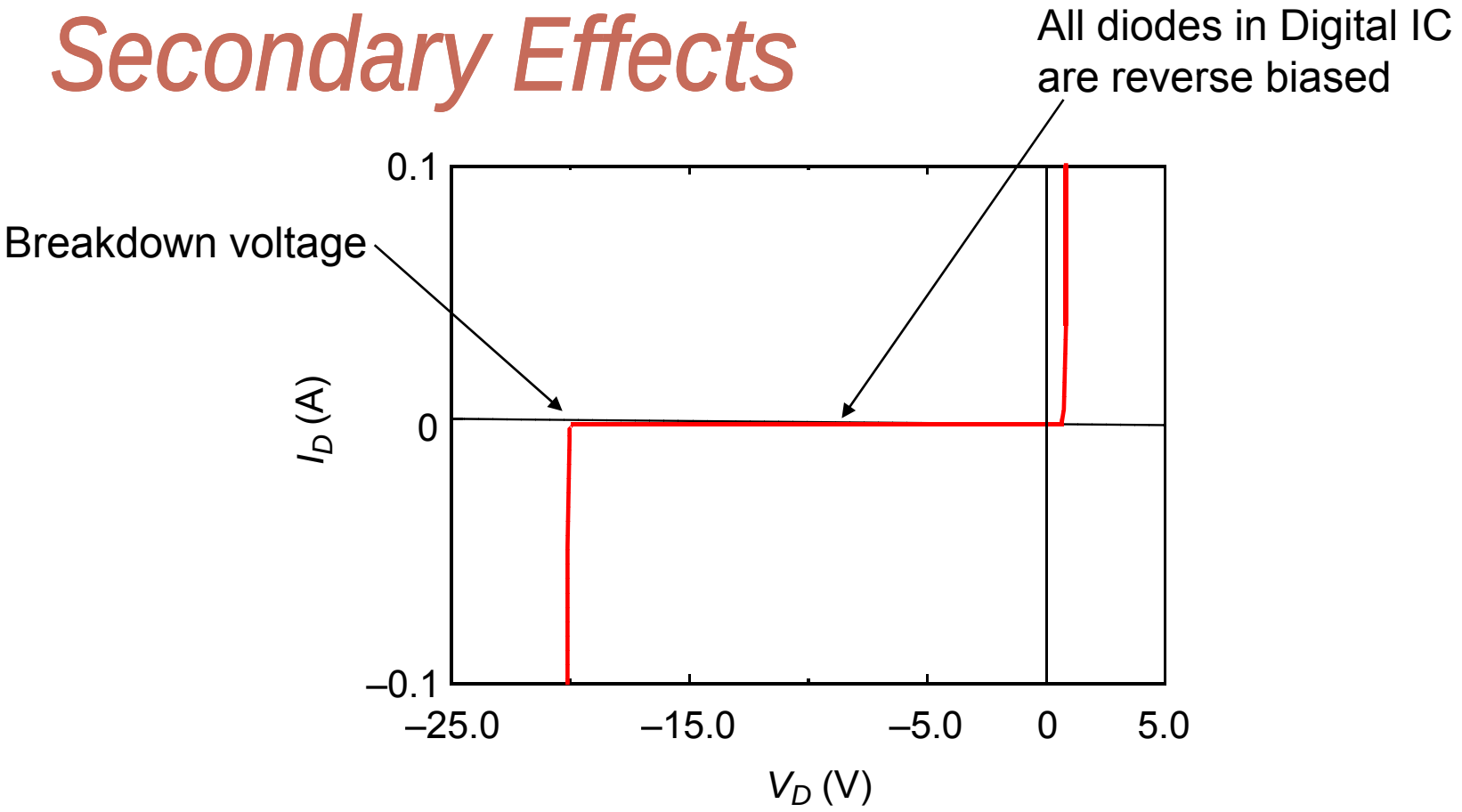


All diodes in Digital IC are reverse biased

$$C_j = \frac{C_{j0}}{(1 - V_D/\phi_0)^m}$$

m = 0.5: abrupt junction
m = 0.33: linear junction

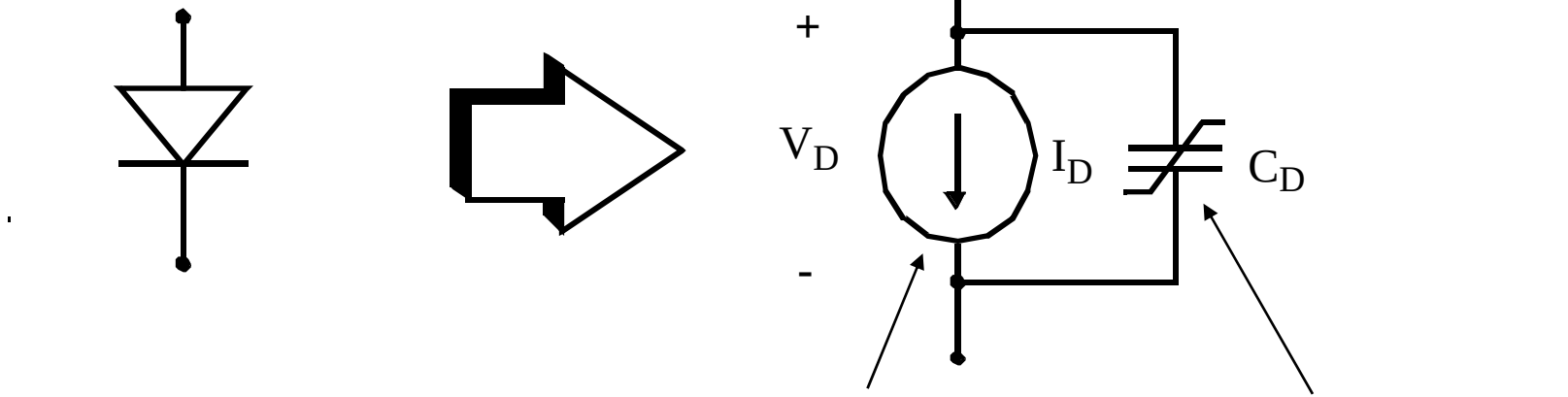
Secondary Effects



Avalanche Breakdown

High reverse voltage → E-field ↑ → carriers are accelerated to high velocity
→High energy carriers create electron-hole pair in the depletion region
→ carriers increase → currents increase

Diode Model



$$i = I_S(e^{v/nV_T} - 1) \qquad C_D = \frac{C_{j0}}{(1 - V_D/\phi_0)^m} + \frac{\tau_T I_S}{\phi_T} e^{V_D/n\phi_T}$$

SPICE Parameters

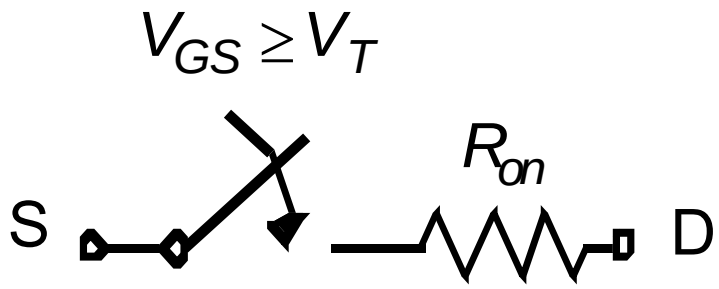
$$i = I_S(e^{v/nV_T} - 1) \qquad C_D = \frac{C_{j0}}{(1 - V_D/\phi_0)^m} + \frac{\tau_T I_S}{\phi_T} e^{V_D/n\phi_T}$$

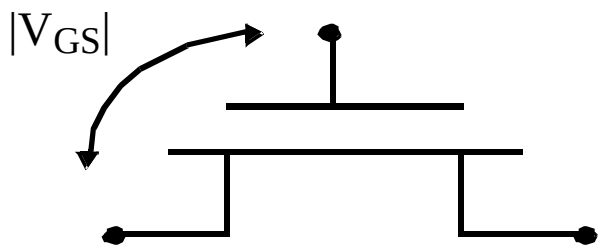
Parameter Name	Symbol	SPICE Name	Units	Default Value
Saturation current	I_S	IS	A	1.0 E-14
Emission coefficient	n	N	-	1
Series resistance	R_S	RS	Ω	0
Transit time	τ_T	TT	sec	0
Zero-bias junction capacitance	C_{j0}	CJ0	F	0
Grading coefficient	m	M	-	0.5
Junction potential	ϕ_0	VJ	V	1

First Order SPICE diode model parameters.

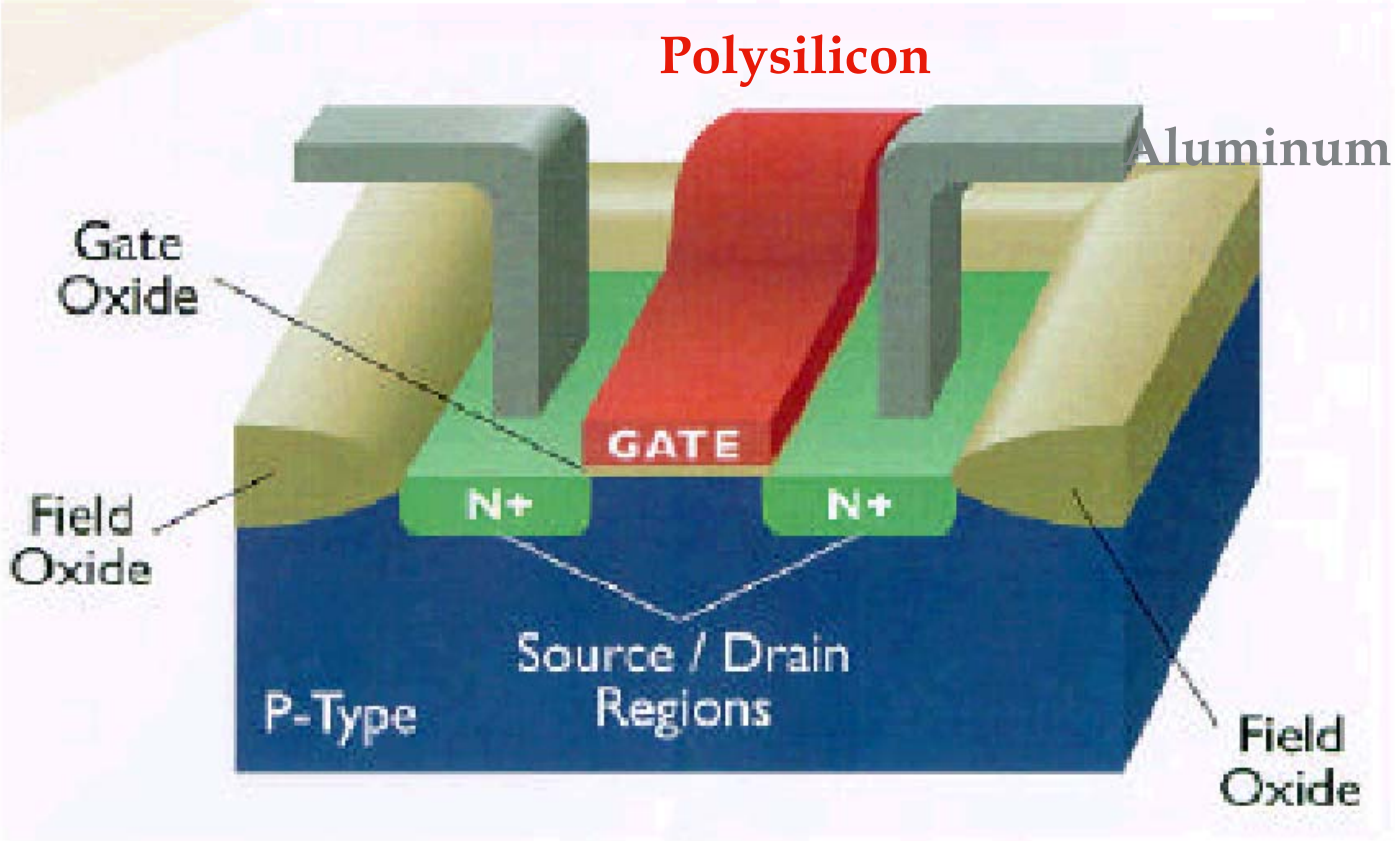
What is a Transistor?

A Switch! ⟷ An MOS Transistor

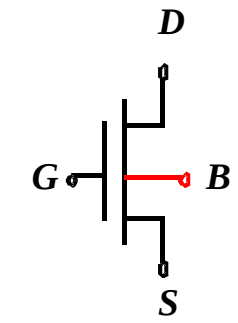




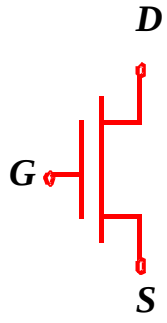
The MOS Transistor



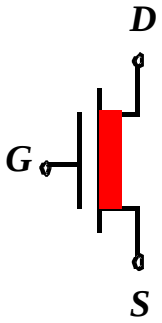
MOS Transistors -Types and Symbols



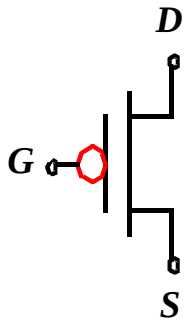
NMOS with Bulk Contact



NMOS Enhancement



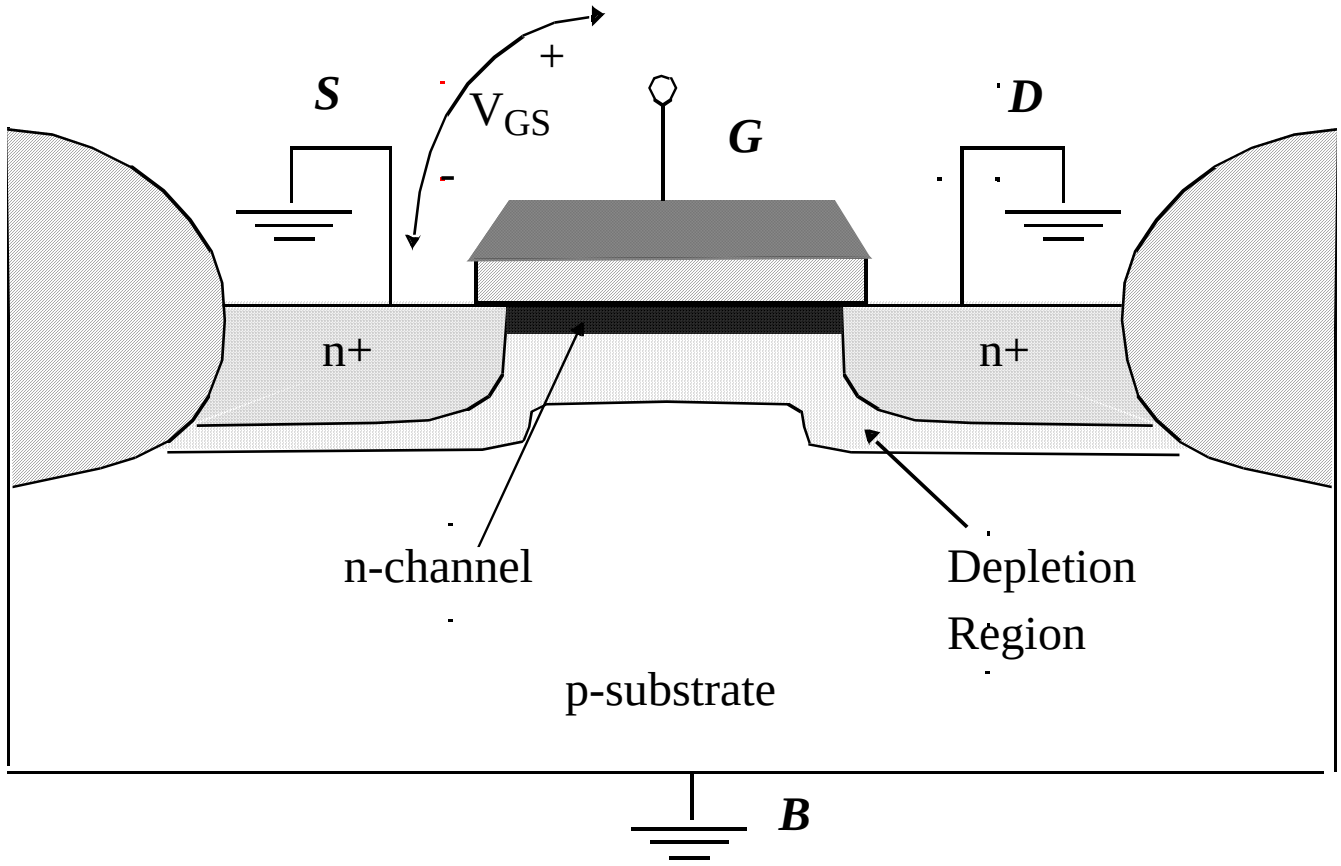
NMOS Depletion



PMOS Enhancement

If the fourth terminal is not shown,
It is assumed that the body is connected to the appropriate supply

Threshold Voltage: Concept



The Threshold Voltage

$$V_T = \phi_{ms} - 2\phi_F - \frac{Q_B}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} - \frac{Q_I}{C_{ox}}$$

Workfunction Difference

Depletion Layer Charge

Surface Charge

Implants

Body Effect Coefficient

$$V_T = V_{T0} + \gamma\left(\sqrt{\left|-2\phi_F + V_{SB}\right|} - \sqrt{\left|-2\phi_F\right|}\right)$$

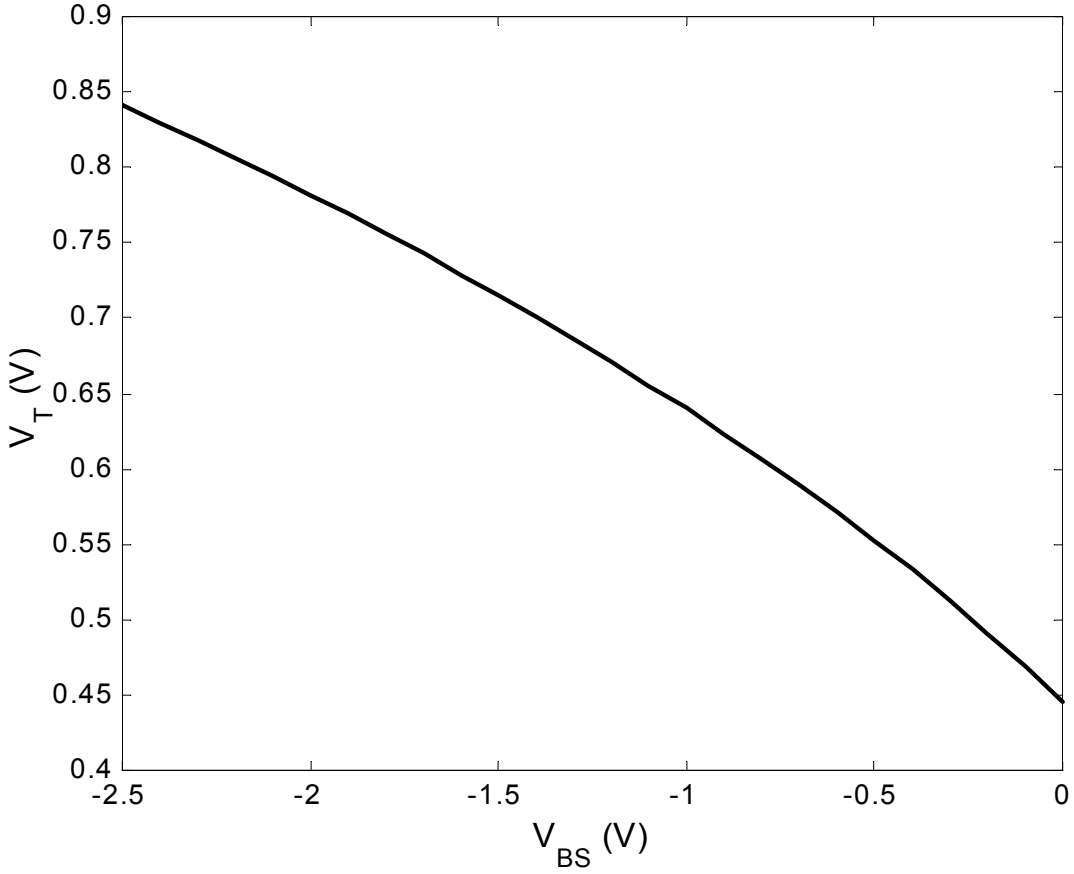
with

$$V_{T0} = \phi_{ms} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} - \frac{Q_I}{C_{ox}}$$

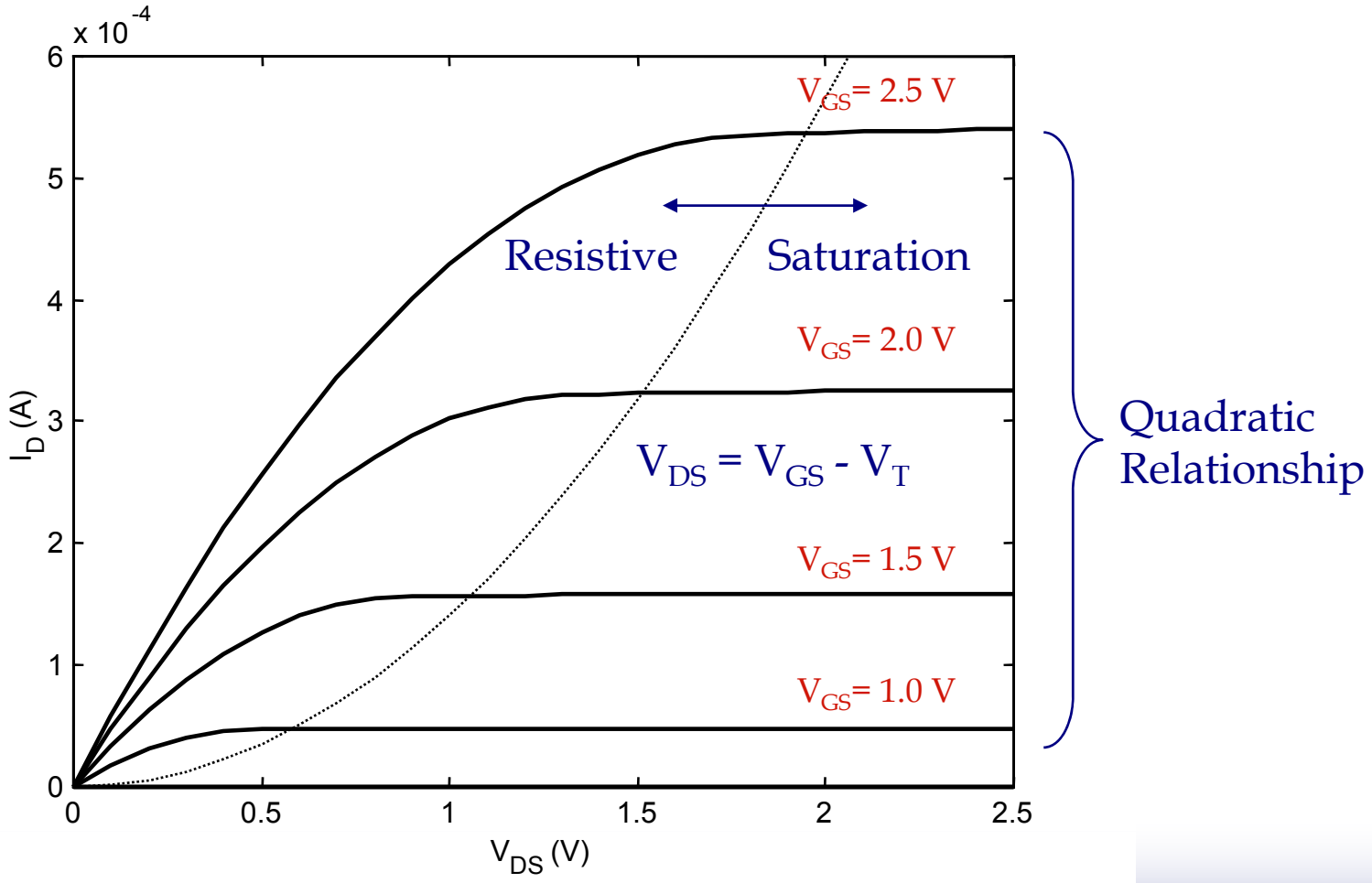
and

$$\gamma = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}}$$

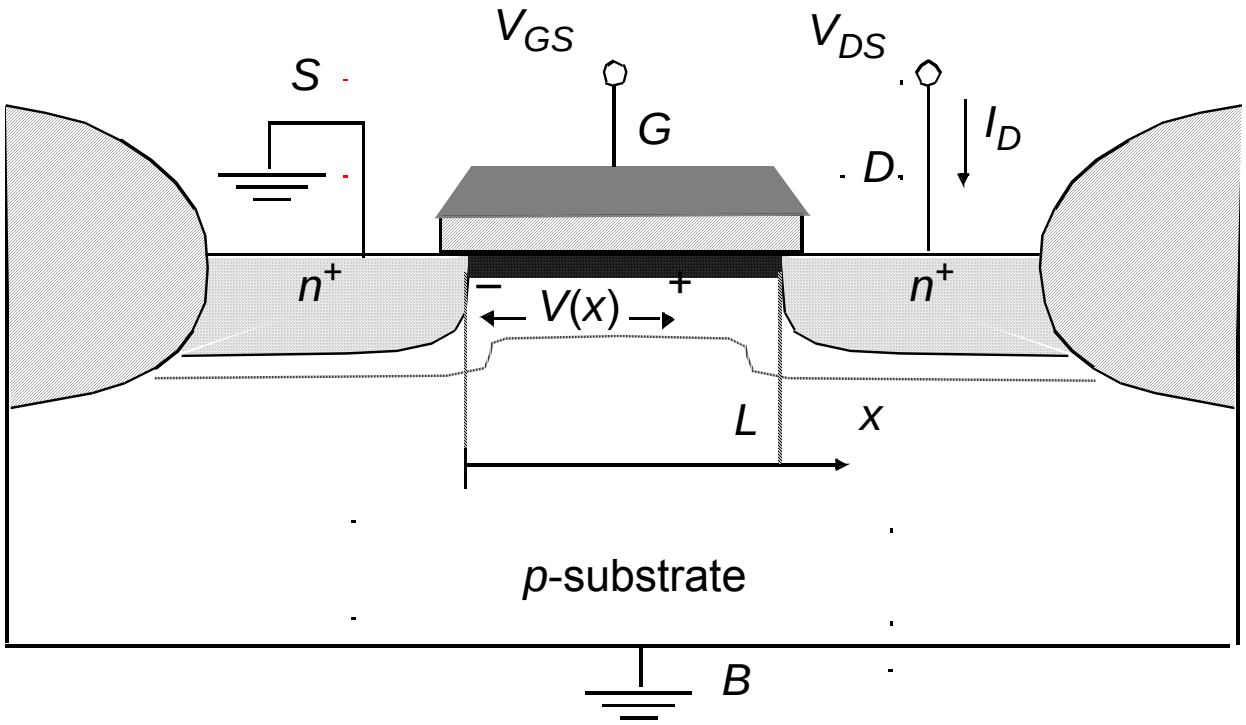
The Body Effect



Current-Voltage Relations

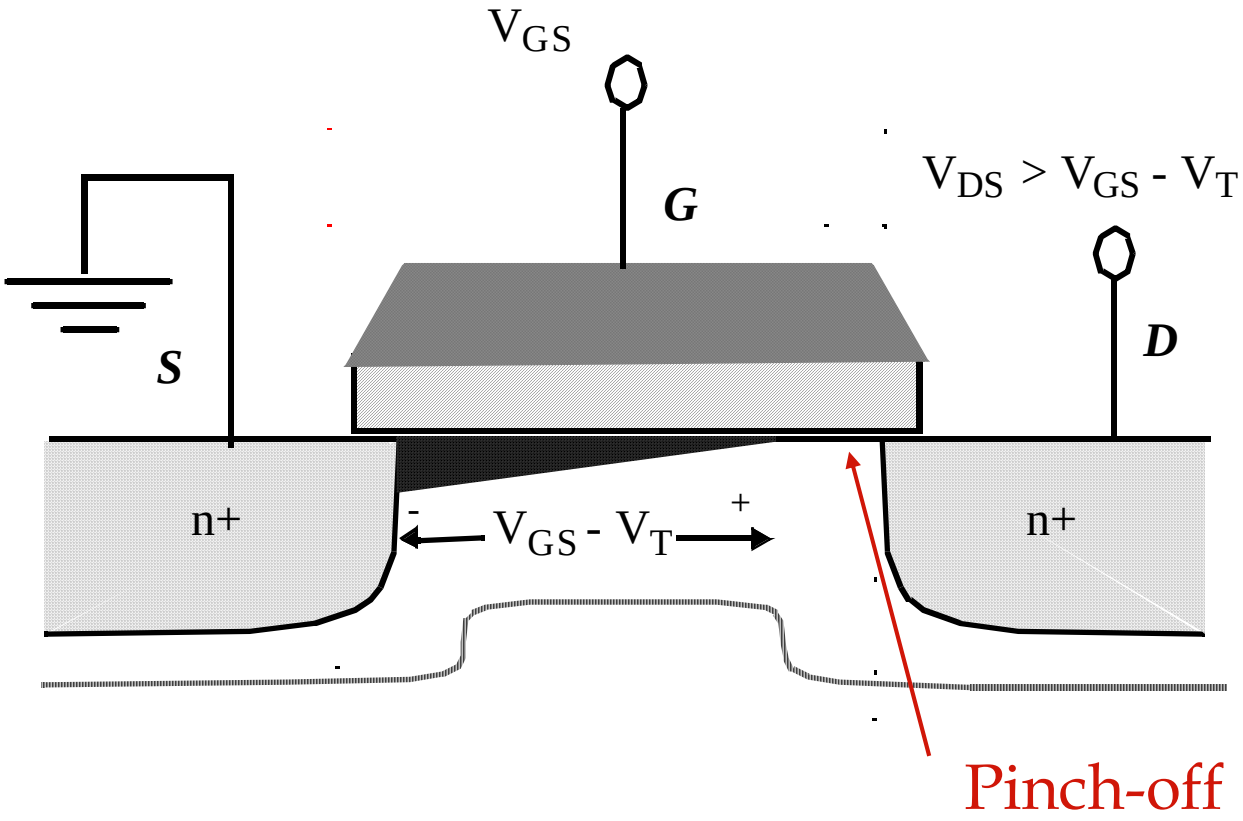


Transistor in Linear



MOS transistor and its bias conditions

Transistor in Saturation



Current-Voltage Relations
Long-Channel Device

Linear Region: $V_{DS} \leq V_{GS} - V_T$

$$I_D = k'_n \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right)$$

with

$$k'_n = \mu_n C_{ox} = \frac{\mu_n \varepsilon_{ox}}{t_{ox}}$$

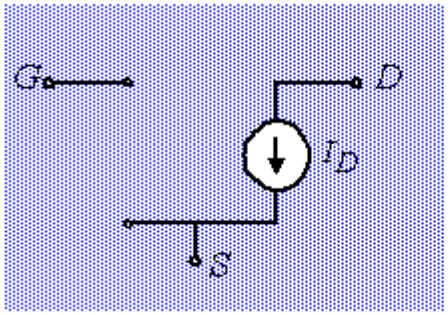
Process Transconductance Parameter

Saturation Mode: $V_{DS} \geq V_{GS} - V_T$

Channel Length Modulation

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

A model for manual analysis



$$V_{DS} > V_{GS} - V_T$$

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

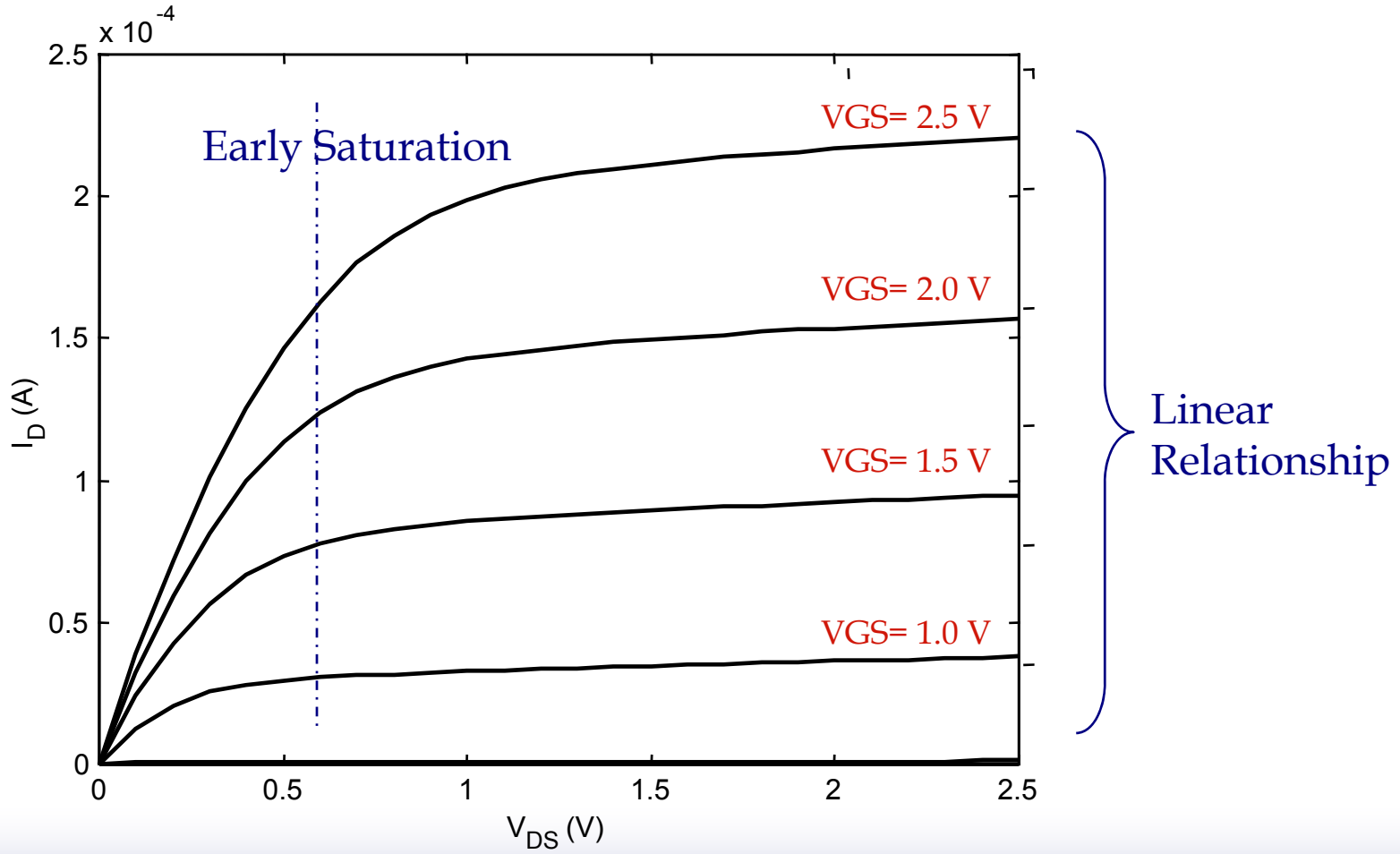
$$V_{DS} < V_{GS} - V_T$$

$$I_D = k'_n \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right)$$

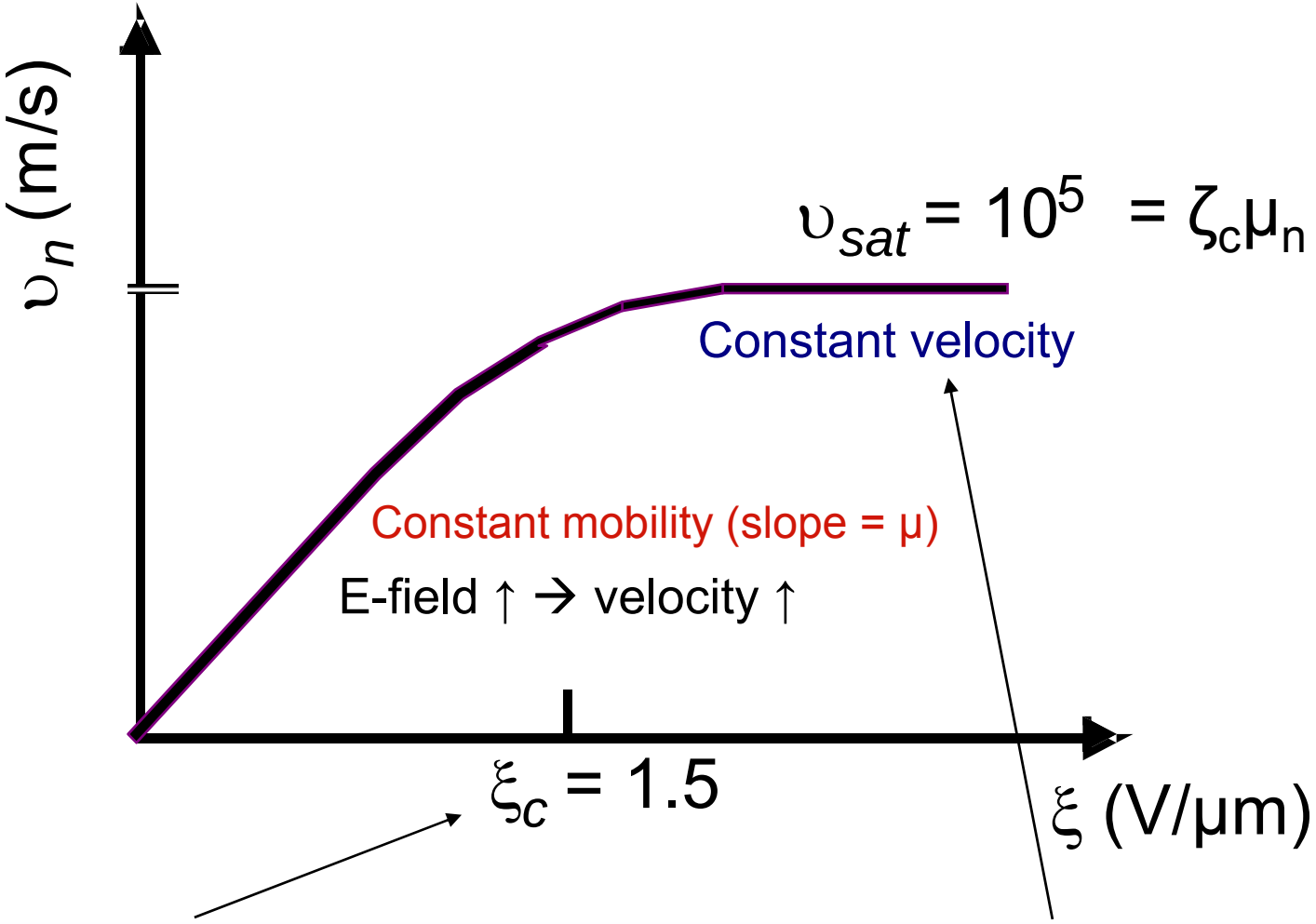
with

$$V_T = V_{T0} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}\right)$$

Current-Voltage Relations
Deep-Submicron Era (Short Channel Devices)

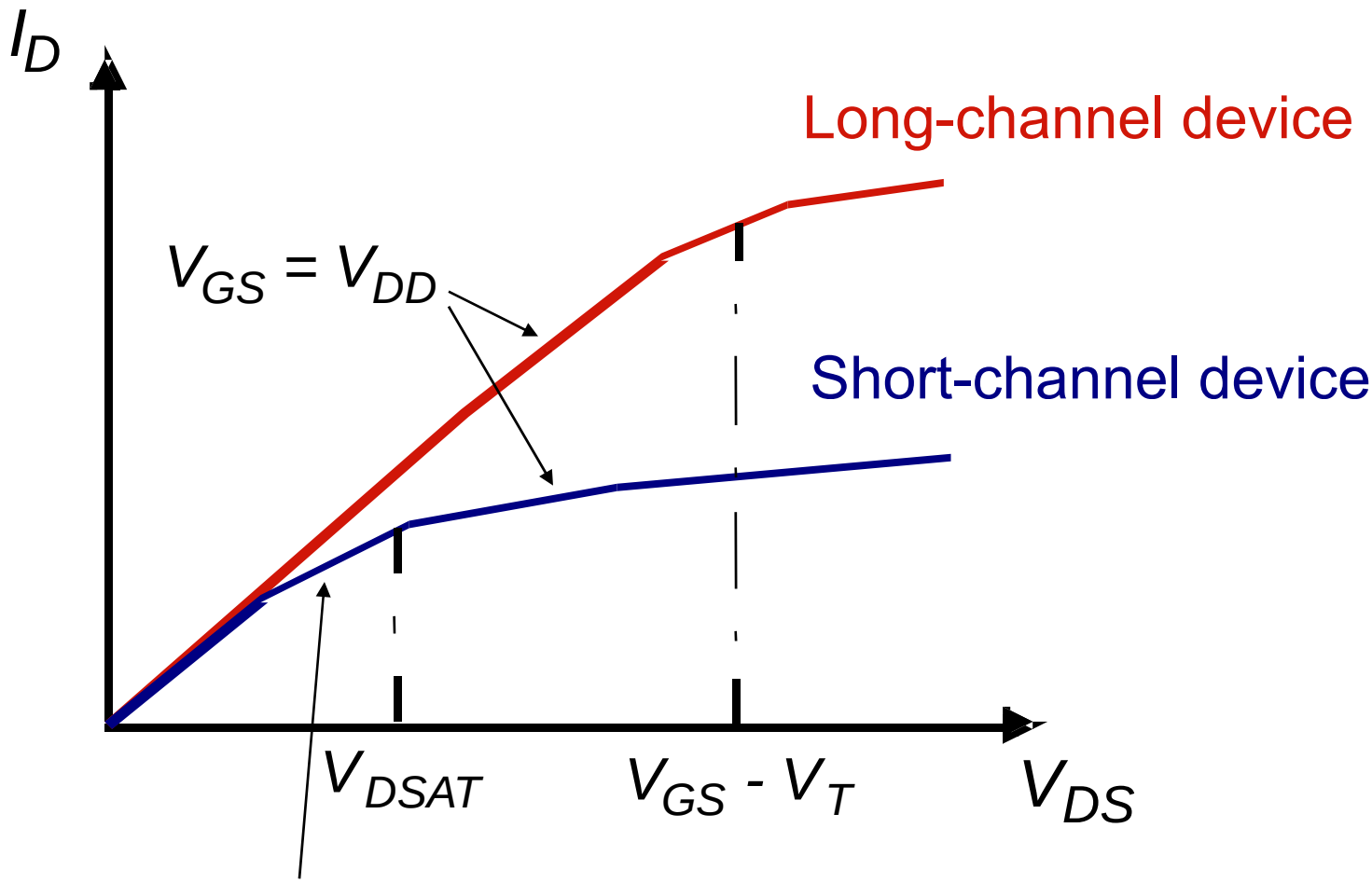


Velocity Saturation



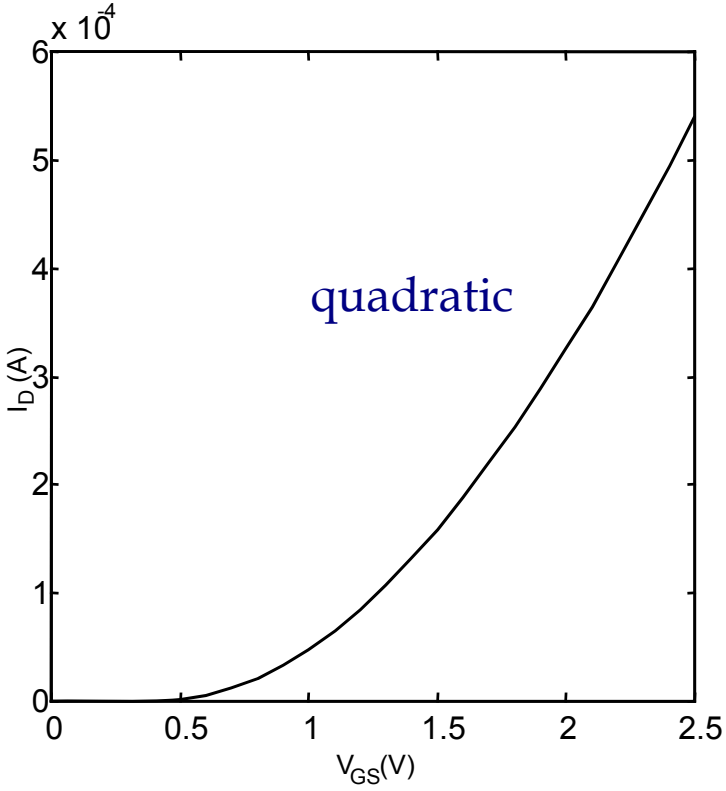
E-field ↑ → critical value → carrier velocity saturates due to scattering effect

Perspective

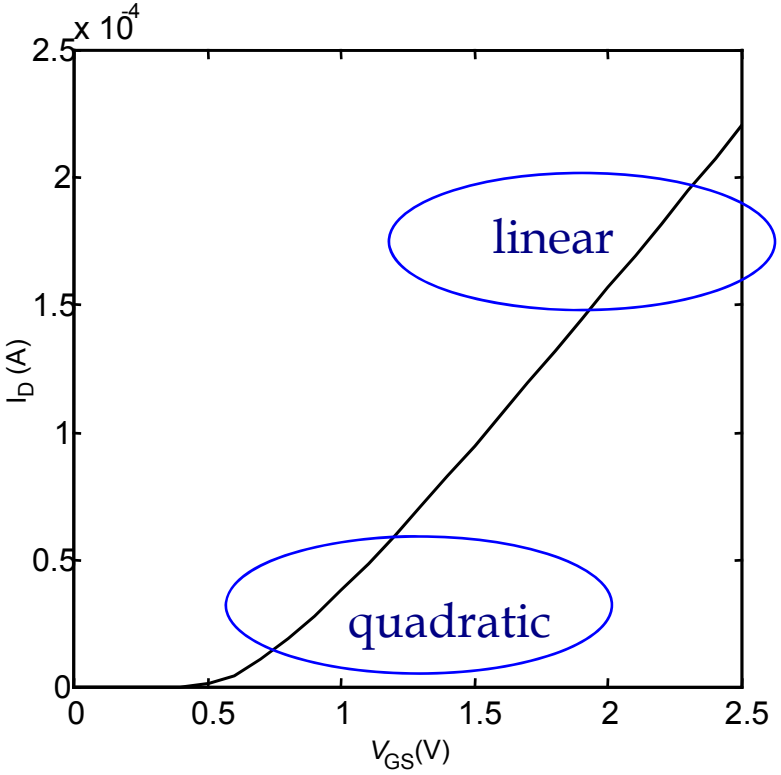


Short channel devices → V_{DD} ↓ → look like long channel devices

I_D versus V_{GS}

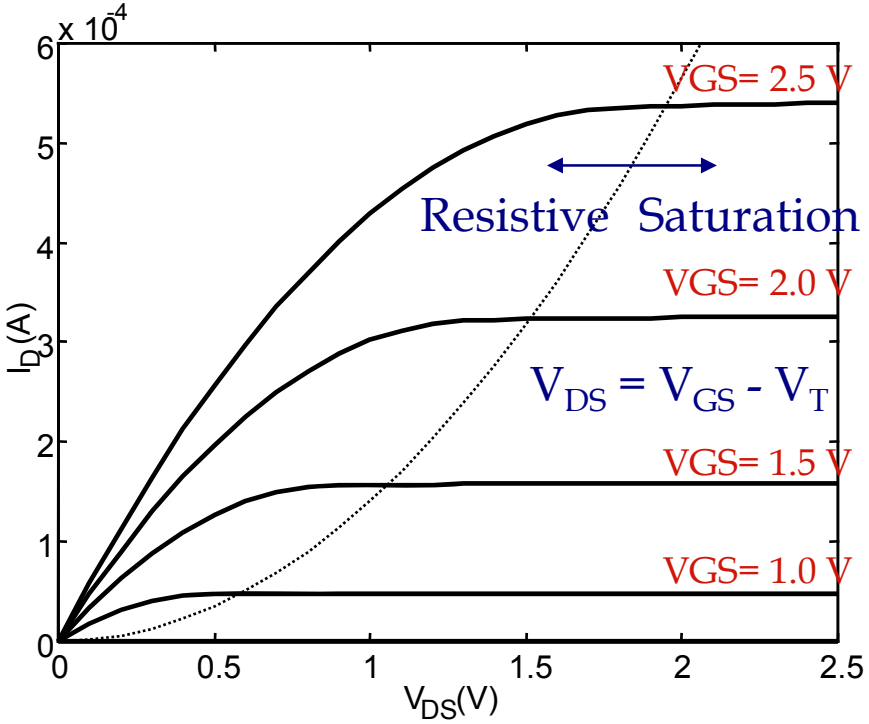


Long Channel

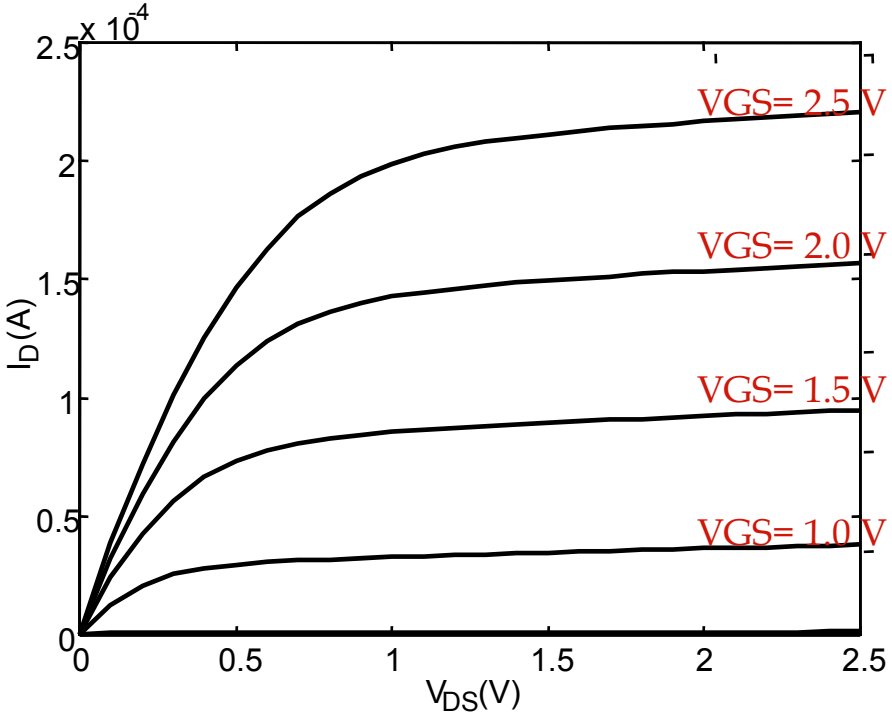


Short Channel

I_D versus V_{DS}

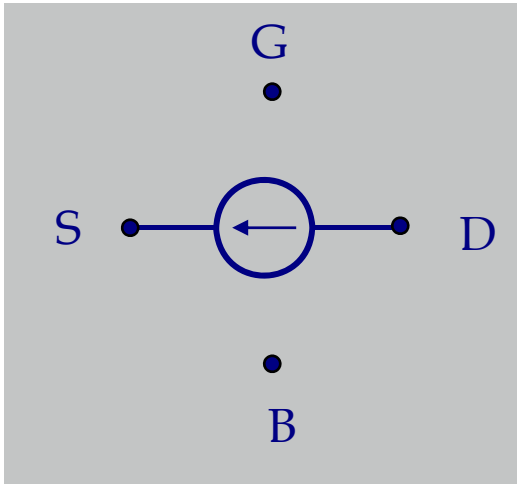


Long Channel



Short Channel

A unified model for manual analysis



$$I_D = 0 \quad \text{for} \quad V_{GT} \leq 0$$

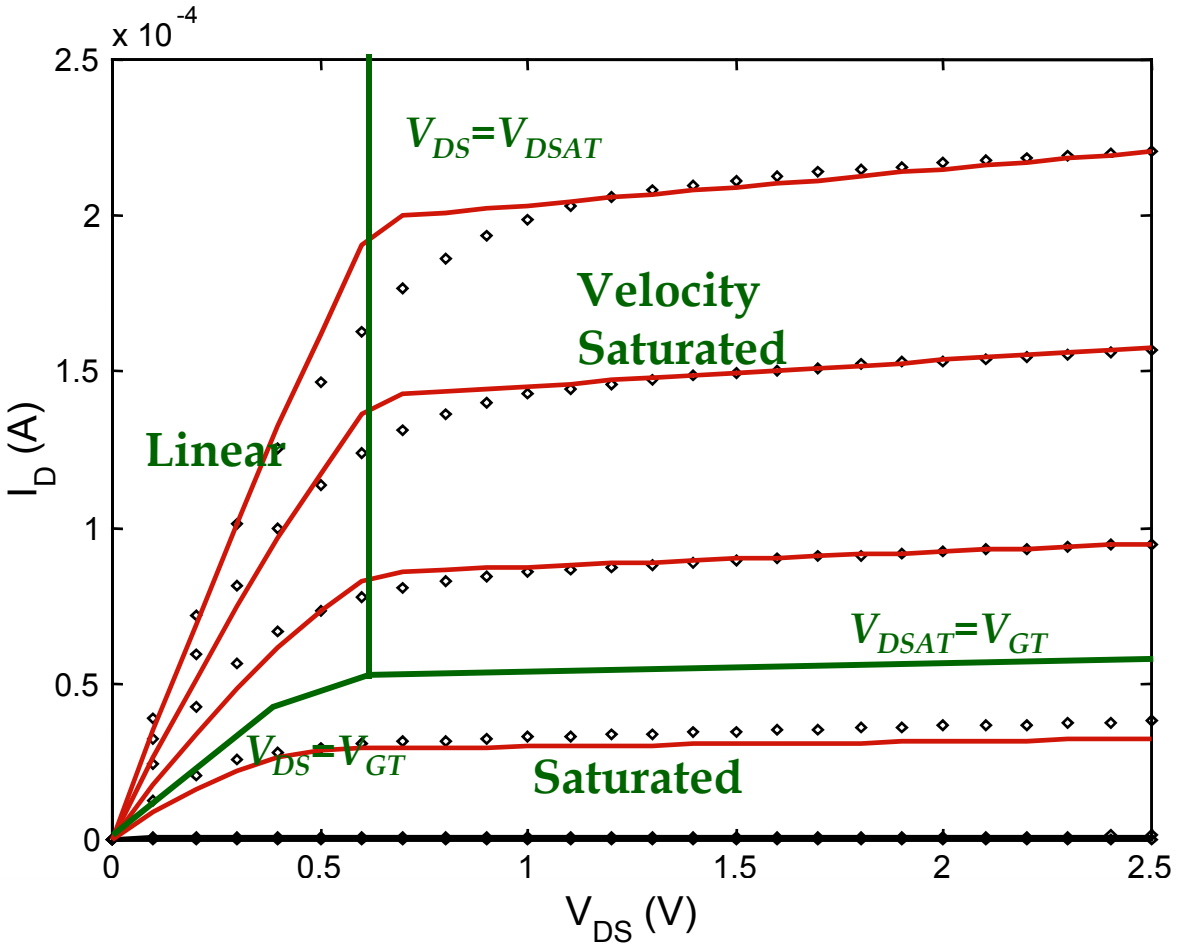
$$I_D = k' \frac{W}{L}\left(V_{GT}V_{min} - \frac{V_{min}^2}{2}\right)(1 + \lambda V_{DS}) \quad \text{for} \quad V_{GT} \geq 0$$

$$\text{with} \quad V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT}),$$

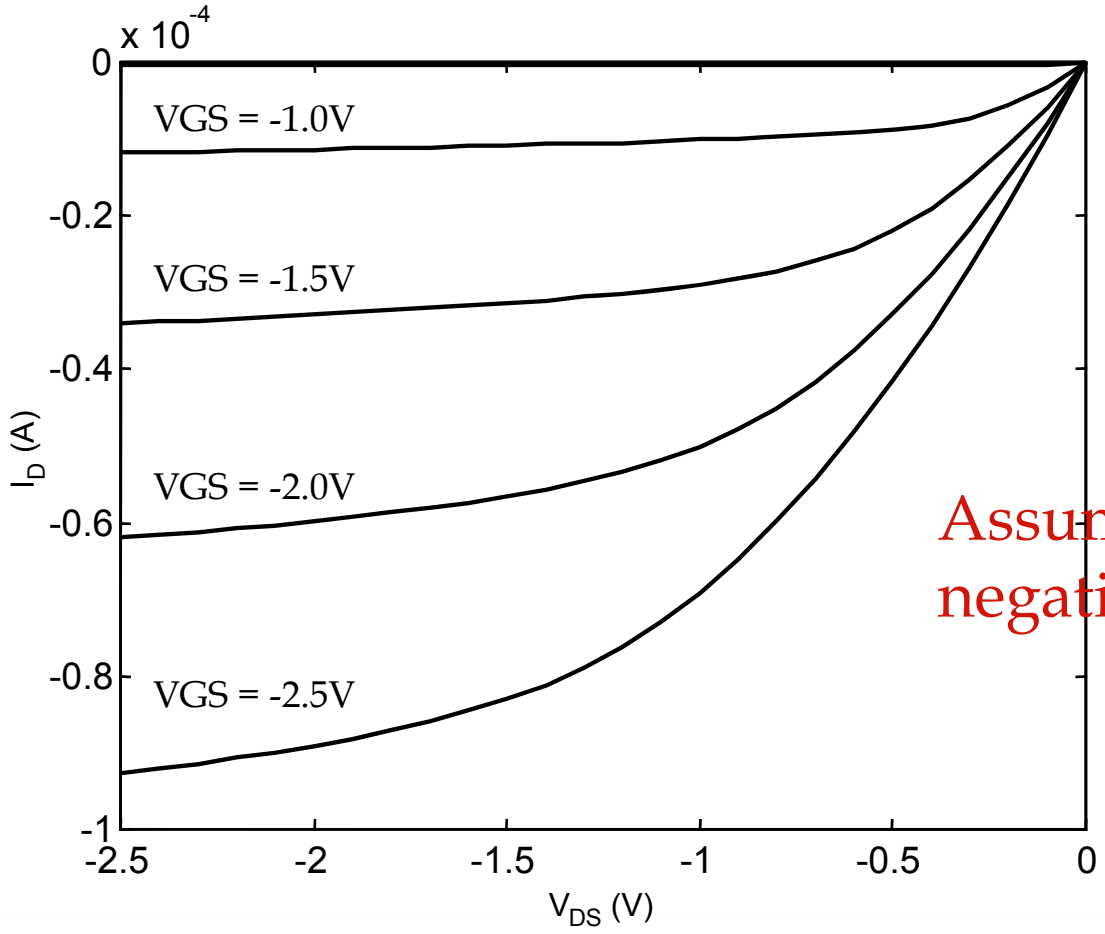
$$V_{GT} = V_{GS} - V_T,$$

$$\text{and} \quad V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

Simple Model versus SPICE



A PMOS Transistor



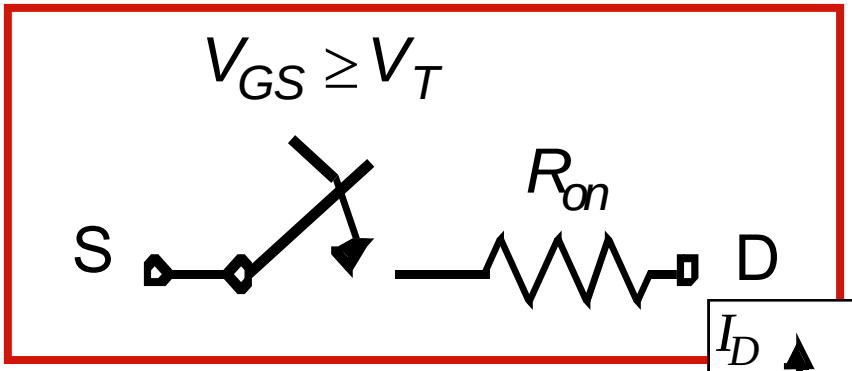
Assume all variables negative!

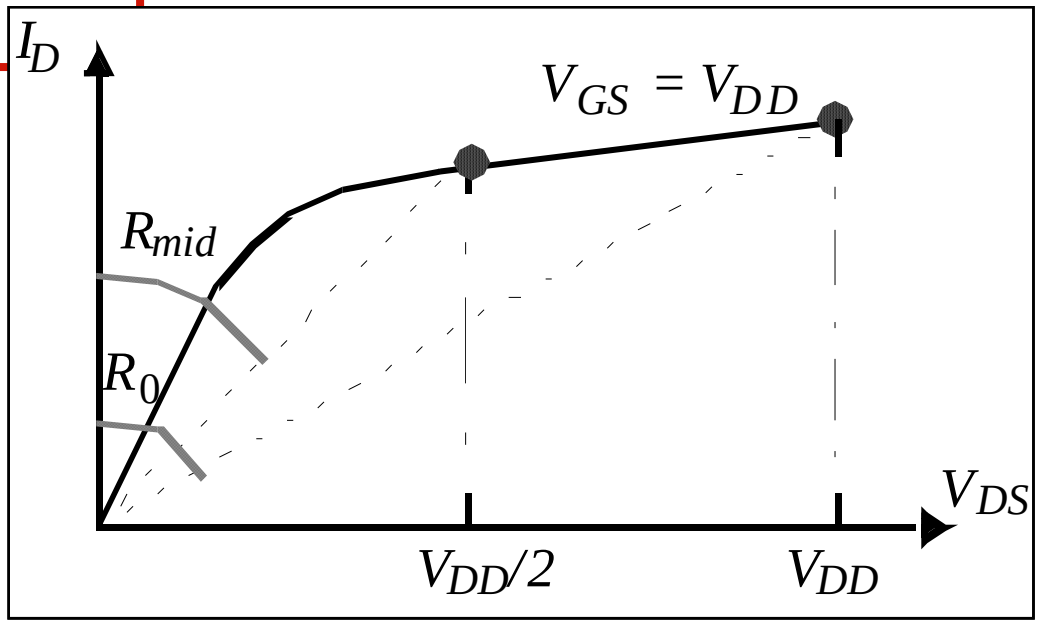
Transistor Model for Manual Analysis

Table 3.2 Parameters for manual model of generic 0.25 μm CMOS process (minimum length device).

	V_{T0} (V)	γ ($V^{0.5}$)	V_{DSAT} (V)	K' (A/V^2)	λ (V^{-1})
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	−0.4	-0.4	-1	-30×10^{-6}	-0.1

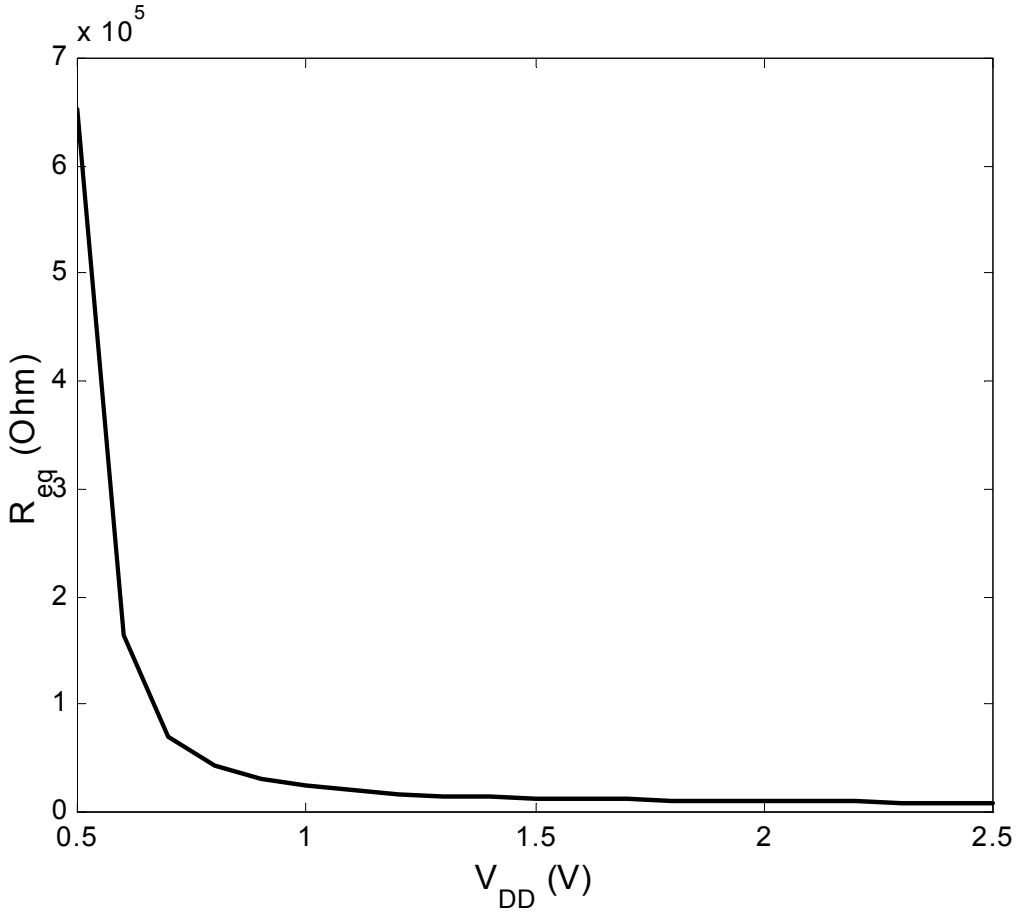
The Transistor as a Switch





$$R_{eq} = \frac{1}{2}\left(\frac{V_{DD}}{I_{DSAT}(1+\lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1+\lambda V_{DD}/2)}\right) \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1-\frac{5}{6}\lambda V_{DD}\right)$$

The Transistor as a Switch



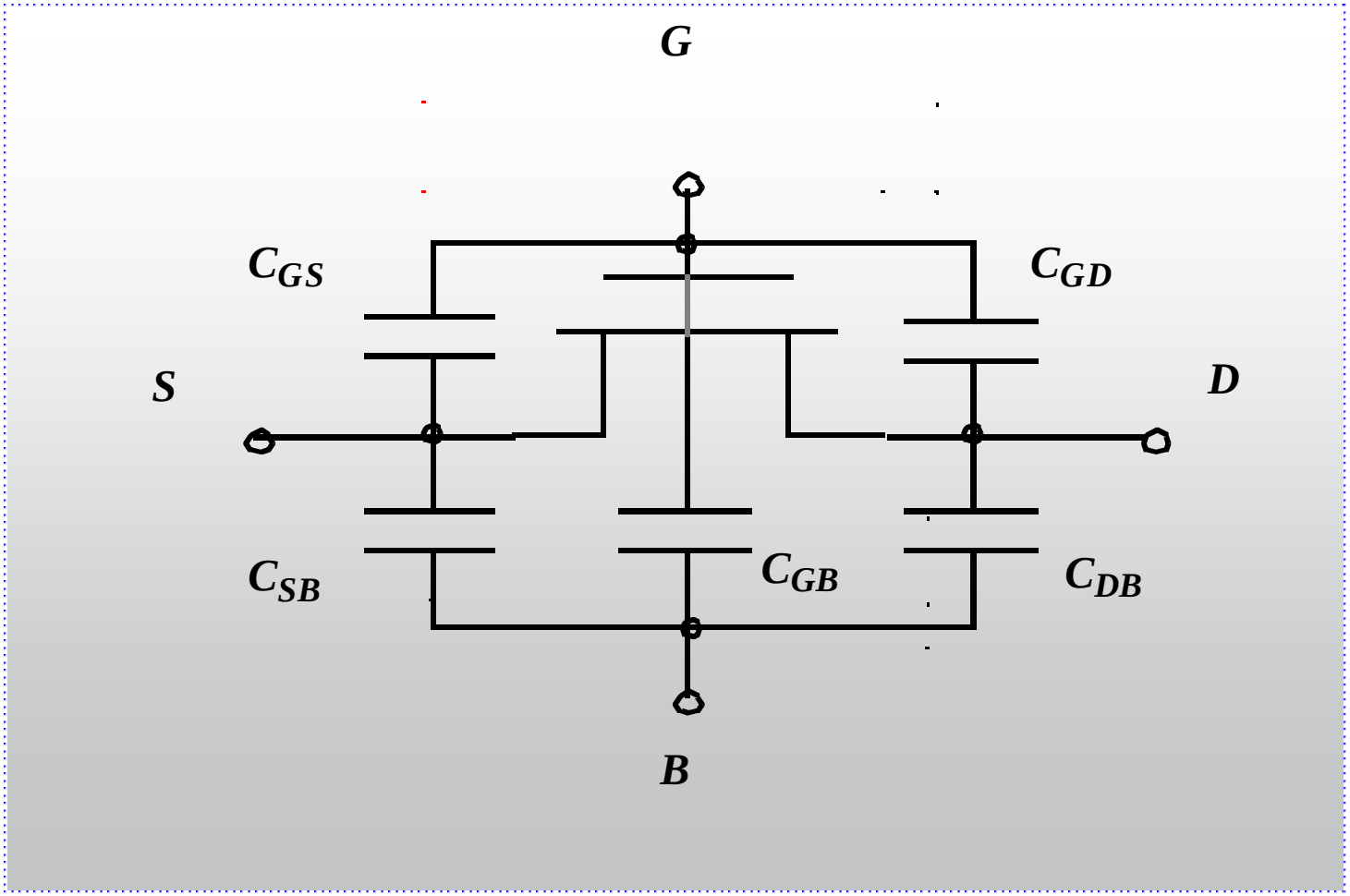
The Transistor as a Switch

Table 3.3 Equivalent resistance R_{eq} (W/L= 1) of NMOS and PMOS transistors in 0.25 μm CMOS process (with $L = L_{min}$). For larger devices, divide R_{eq} by W/L.

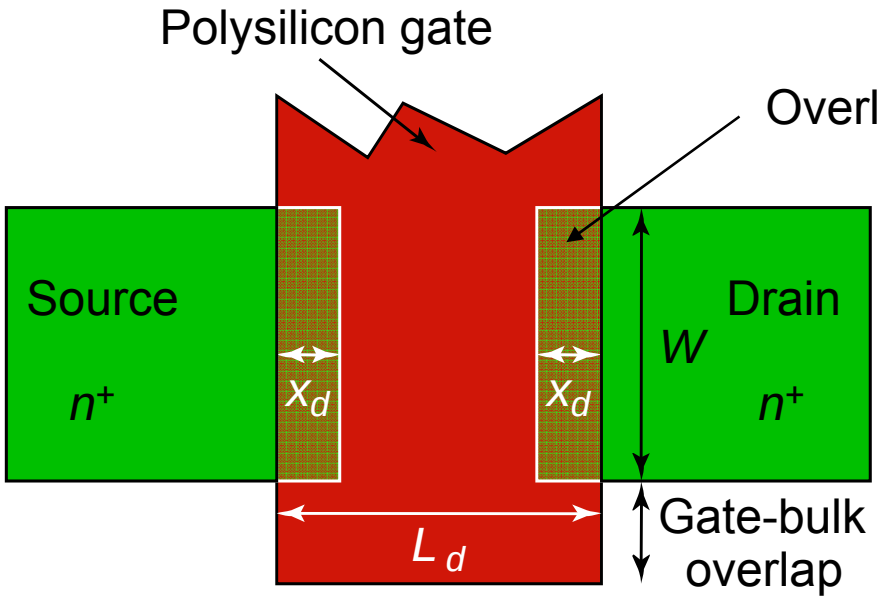
V_{DD} (V)	1	1.5	2	2.5
NMOS (kΩ)	35	19	15	13
PMOS (kΩ)	115	55	38	31

MOS Capacitances
Dynamic Behavior

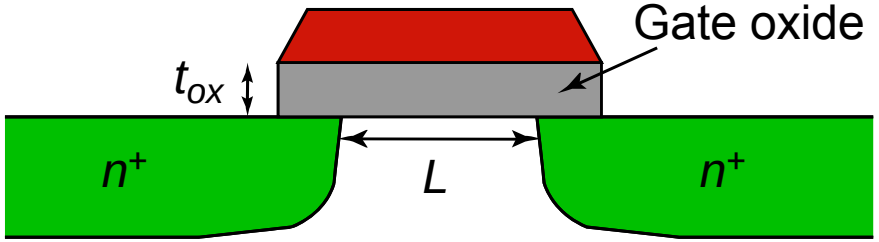
Dynamic Behavior of MOS Transistor



The Gate Capacitance



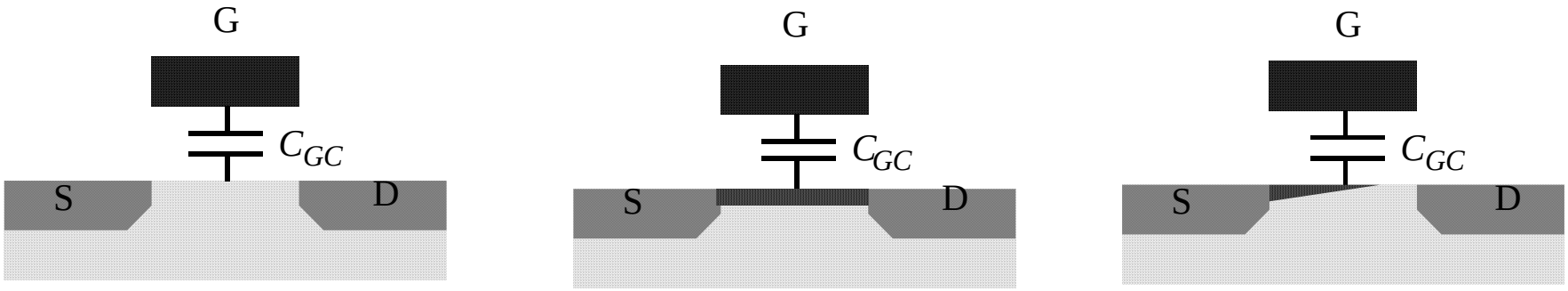
Top view



Cross section

$$C_{gate} = \frac{\varepsilon_{ox}}{t_{ox}} WL$$

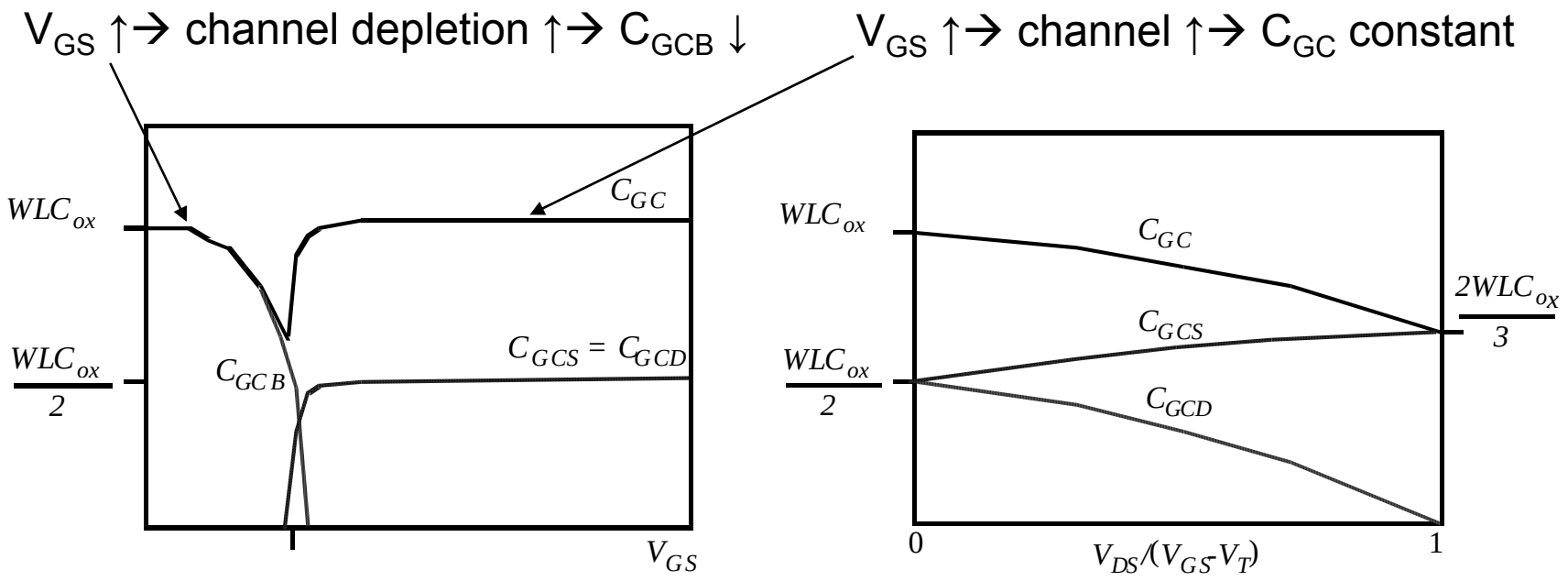
Gate Capacitance



Operation Region	C_{gb}	C_{gs}	C_{gd}
Cutoff	$C_{ox}WL_{eff}$	0	0
Triode	0	$C_{ox}WL_{eff}/2$	$C_{ox}WL_{eff}/2$
Saturation	0	$(2/3)C_{ox}WL_{eff}$	0

Most important regions in digital design: saturation and cut-off

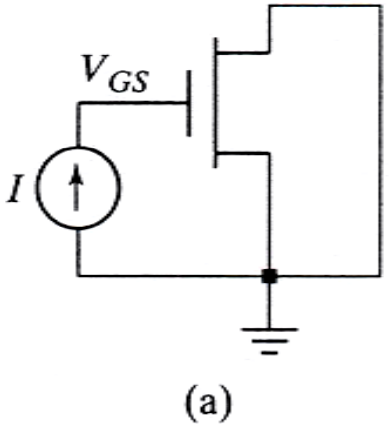
Gate Capacitance



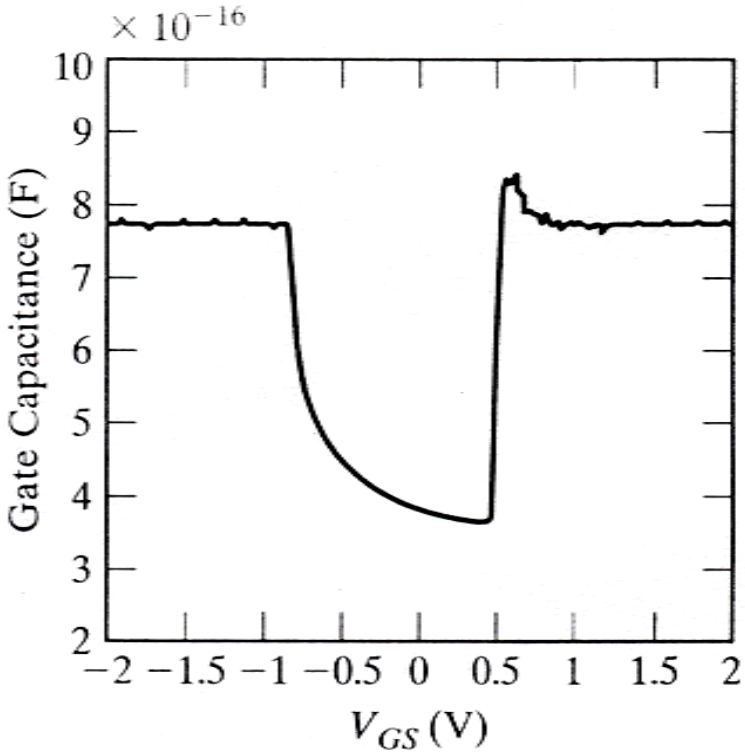
Capacitance as a function of V_{GS} (with $V_{DS} = 0$)

Capacitance as a function of the degree of saturation

Measuring the Gate Cap



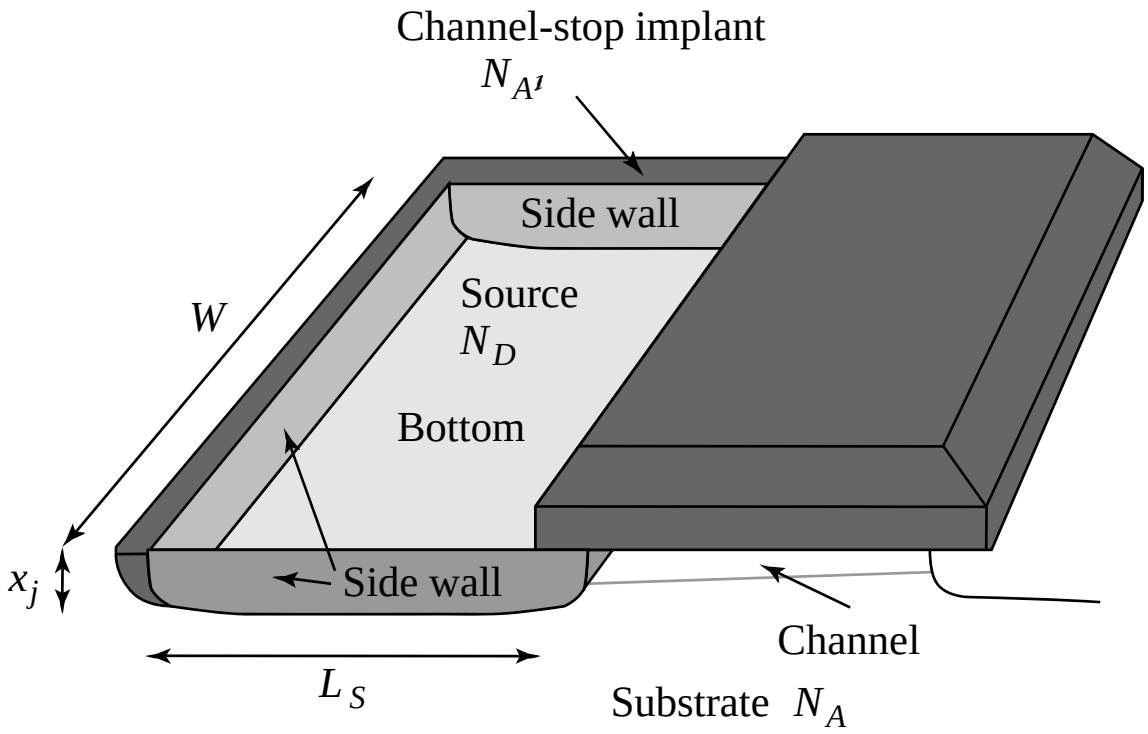
(a)



$$I = C_G(V_{GS})\frac{dV_{GS}}{dt}$$

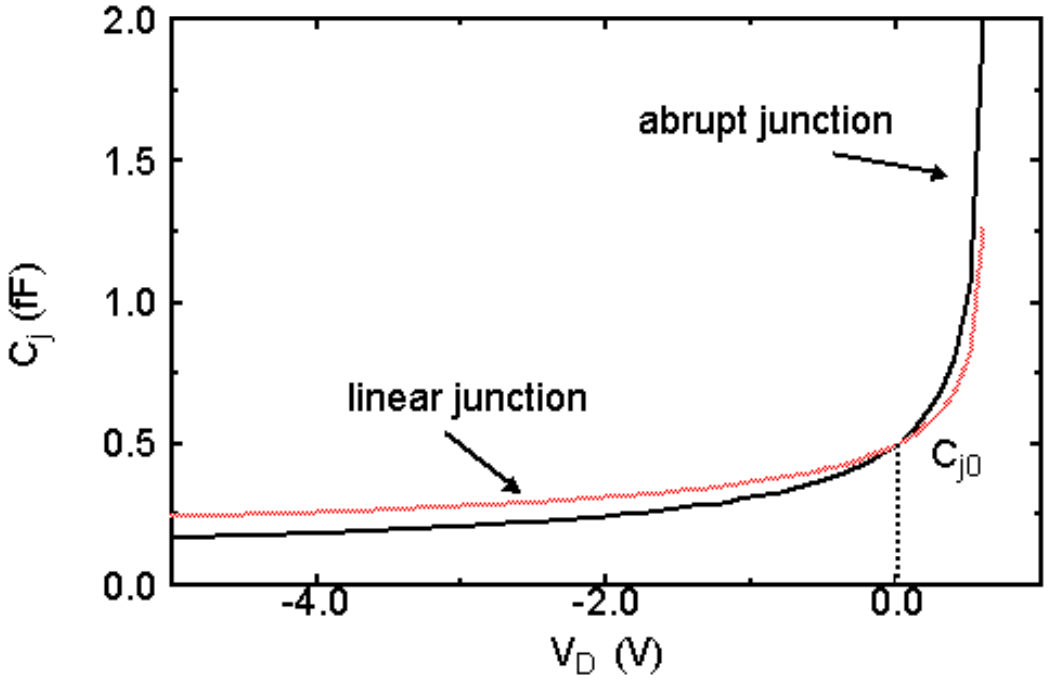
$$C_G(V_{GS}) = I / \frac{dV_{GS}}{dt}$$

Diffusion Capacitance (Junction Cap.)



$$C_{diff} = C_{bottom} + C_{sw} = C_j \times AREA + C_{jsw} \times PERIMETER$$
$$= C_j L_S W + C_{jsw}(2L_S + W)$$

Junction Capacitance



$$C_j = \frac{C_{j0}}{(1 - V_D/\phi_0)^m}$$

m = 0.5: abrupt junction
m = 0.33: linear junction

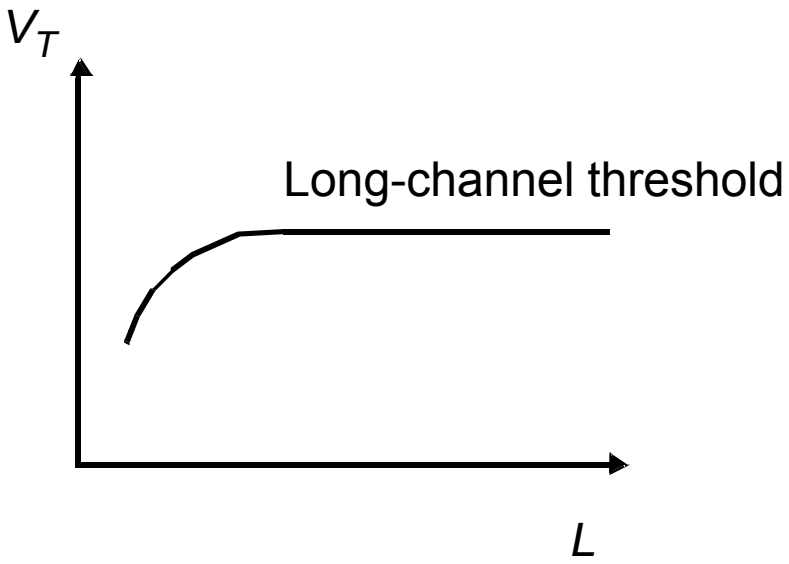
Capacitances in 0.25 μm CMOS process

	C_{ox} (fF/μm^2)	C_O (fF/μm)	C_j (fF/μm^2)	m_j	ϕ_b (V)	C_{jsw} (fF/μm)	m_{jsw}	ϕ_{bsw} (V)
NMOS	6	0.31	2	0.5	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9

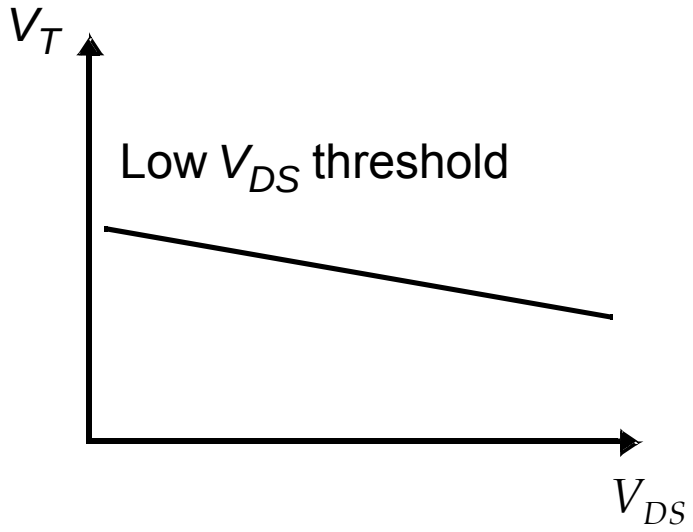
The Sub-Micron MOS Transistor

- **Threshold Variations**
- **Subthreshold Conduction**
- **Parasitic Resistances**

Threshold Variations



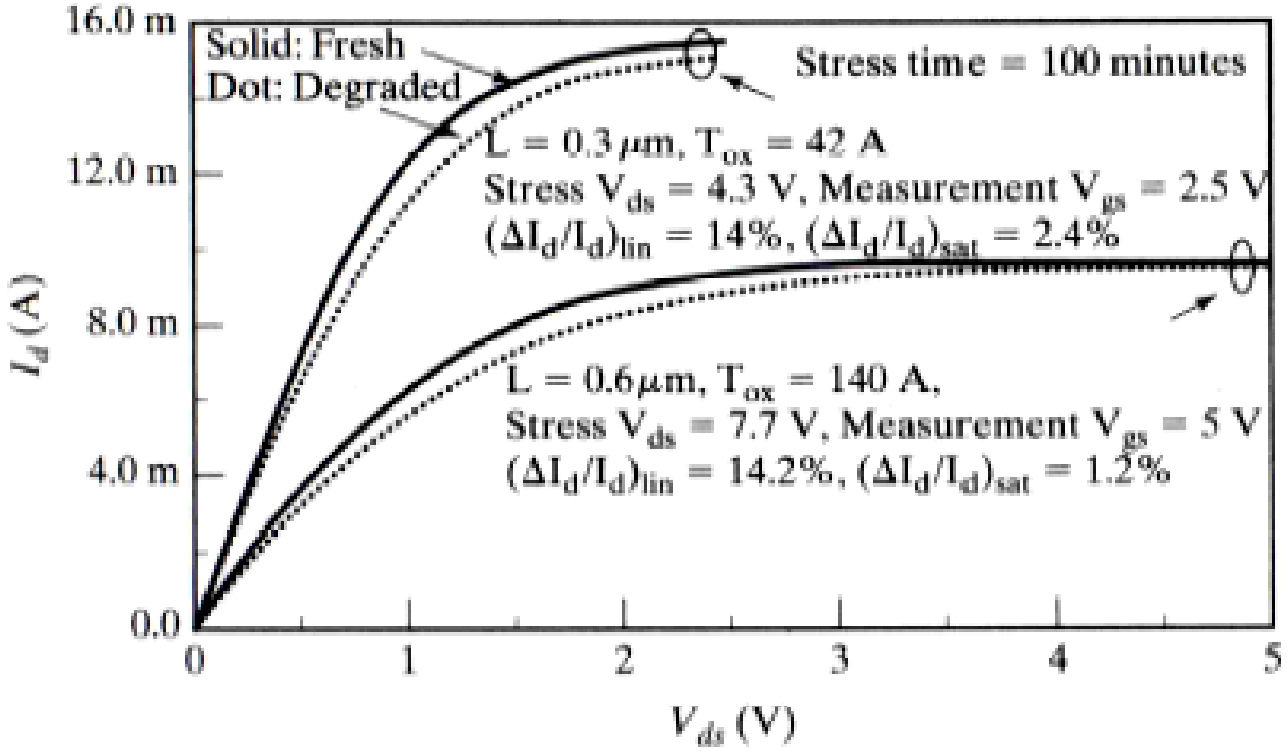
Threshold as a function of the length (for low V_{DS})



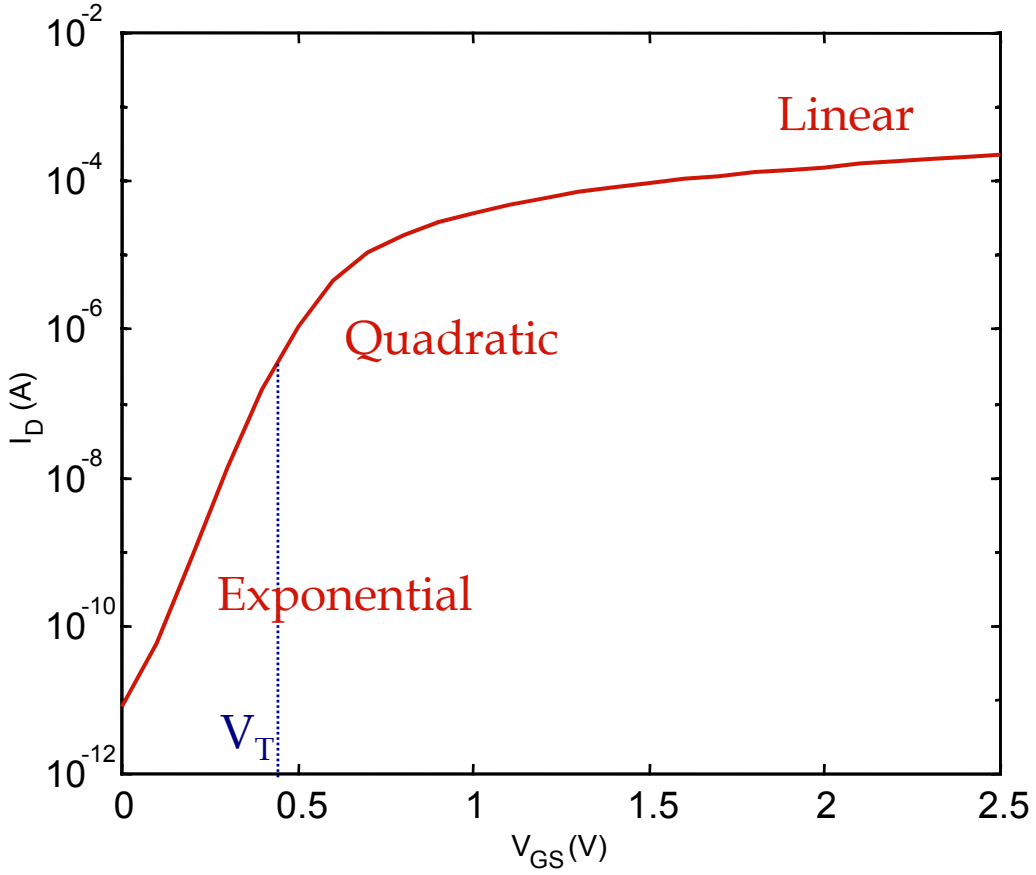
Drain-induced barrier lowering (DIBL) (for low L)

Short channel effect?
Narrow channel effect?
Drain-induced barrier lowering (DIBL)?
Punch-through?

Hot carrier effect



Sub-Threshold Conduction



The Slope Factor

$$I_D \sim I_0 e^{\frac{qV_{GS}}{nkT}}, \quad n = 1 + \frac{C_D}{C_{ox}}$$

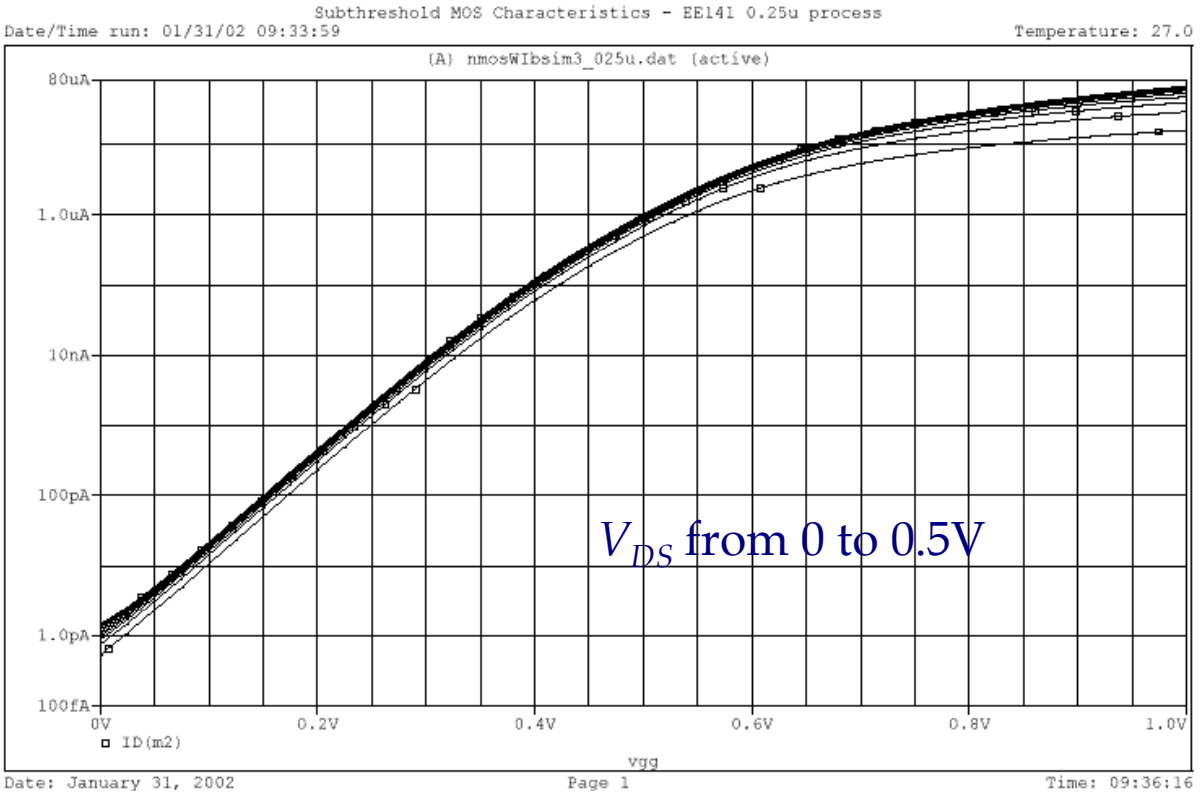
S is ΔV_{GS} for I_{D2}/I_{D1} =10

$$S = n\left(\frac{kT}{q}\right)\ln(10)$$

Typical values for S:
60 .. 100 mV/decade

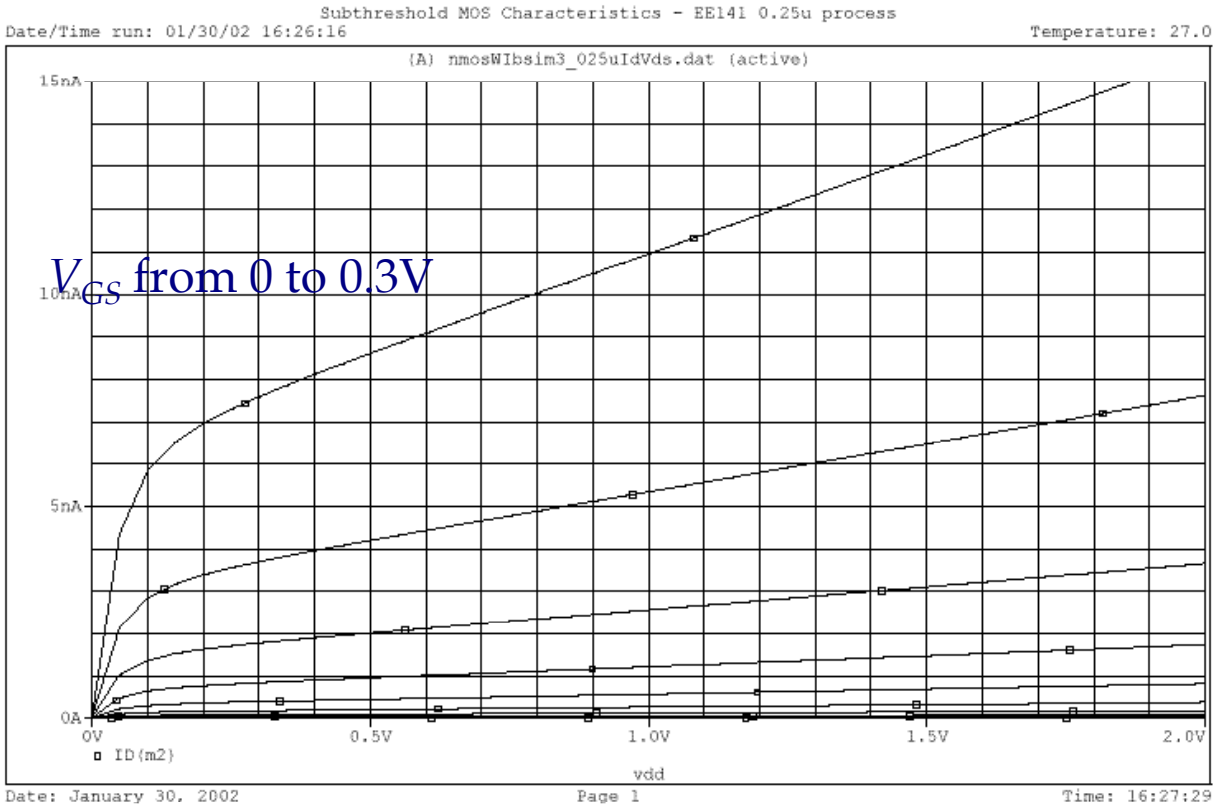
Sub-Threshold I_D *vs* V_{GS}

$$I_D = I_0 e^{\frac{qV_{GS}}{nkT}} \left(1 - e^{-\frac{qV_{DS}}{kT}}\right)$$



Sub-Threshold I_D vs V_{DS}

$$I_D = I_0 e^{\frac{qV_{GS}}{nkT}} \left(1 - e^{-\frac{qV_{DS}}{kT}}\right)\left(1 + \lambda \cdot V_{DS}\right)$$



V_{GS} from 0 to 0.3V

Summary of MOSFET Operating Regions

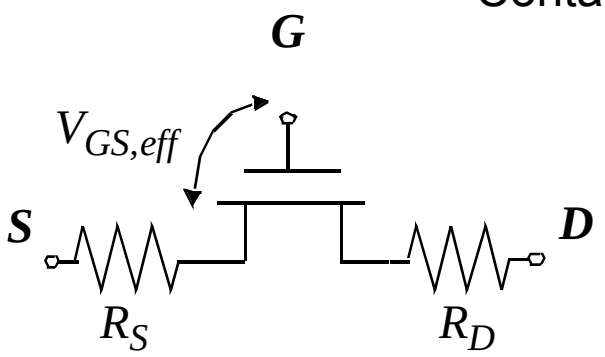
- Strong Inversion $V_{GS} > V_T$
  - Linear (Resistive) $V_{DS} < V_{DSAT}$
  - Saturated (Constant Current) $V_{DS} \geq V_{DSAT}$
- Weak Inversion (Sub-Threshold) $V_{GS} \leq V_T$
  - Exponential in V_{GS} with linear V_{DS} dependence

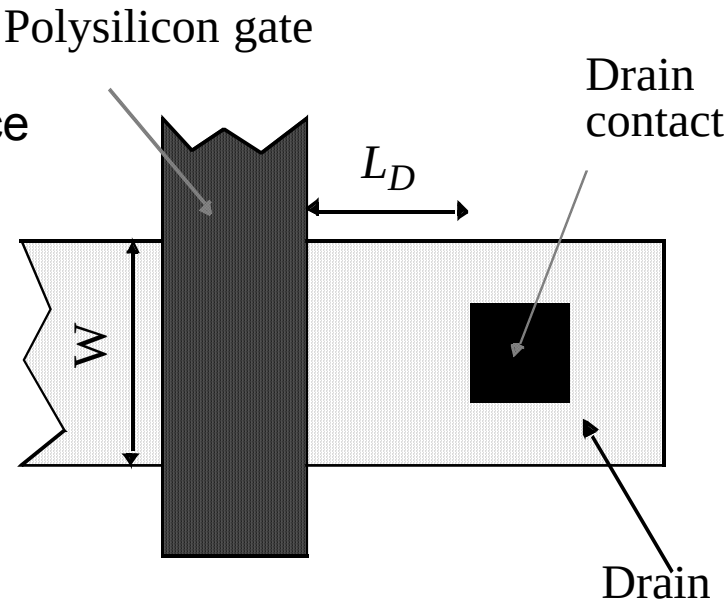
Parasitic Resistances

Sheet Resistance

$$R_{S,D} = \frac{L_{S,D}}{W} R_{sh} + R_C$$

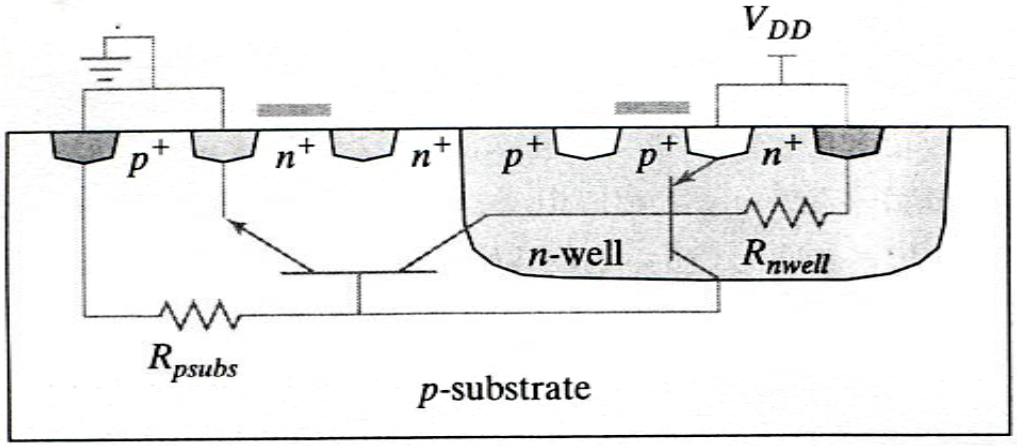
Contact Resistance



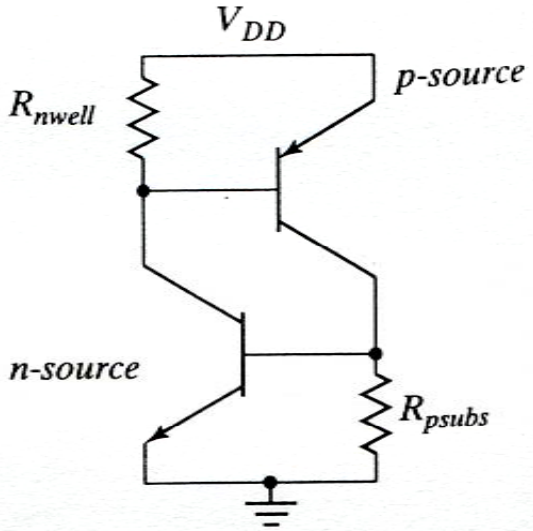


TR. Scale down → shallow junction & small contact → R ↑
Metal over S/D = silicidation → R ↓

Latch-up

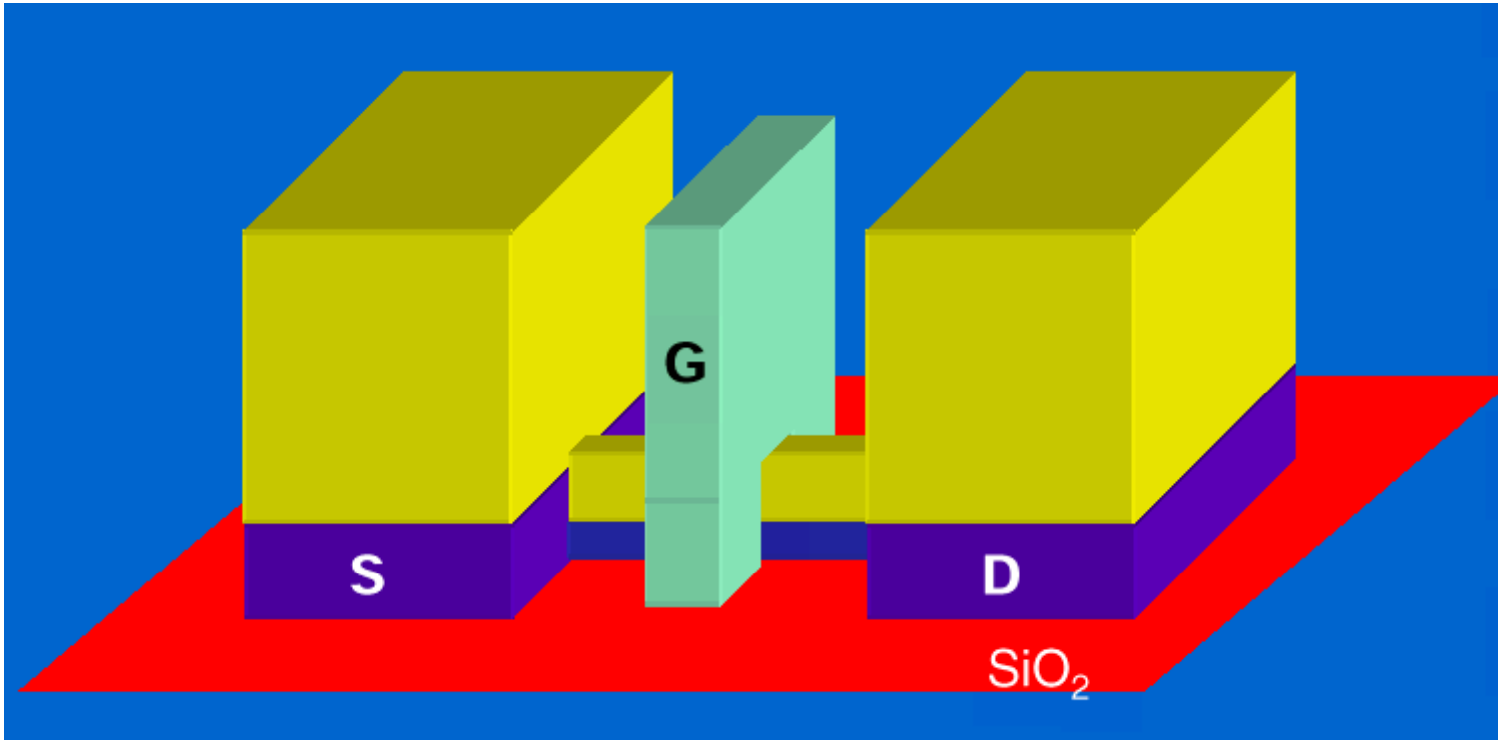


(a) Origin of latchup



(b) Equivalent circuit

Future Perspectives



25 nm FINFET MOS transistor