Design of Analog CMOS Integrated Circuits

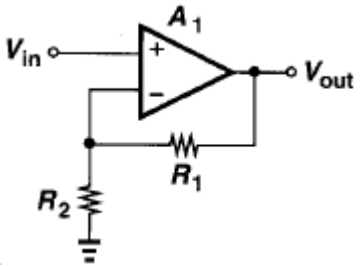
<Chapter 9>

Operational Amplifiers

양병도

9.1 Performance Parameters

- Gain
  - ✓ Open-loop gain은 feedback system에서의 정확도 결정 → High open-loop gain
- Example 9.1
  - ✓ $1 + R_1/R_2 = 10$
  - ✓ Error가 1% 미만이기 위한 A_1?

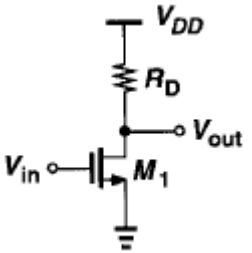


$$\frac{V_{out}}{V_{in}} = \frac{A_1}{1+\frac{R_2}{R_1+R_2}A_1} = \frac{R_1+R_2}{R_2}\cdot\frac{A_1}{\frac{R_1+R_2}{R_2}+A_1}$$

If $A_1 >> (R_1 + R_2)/R_2$, then $\frac{V_{out}}{V_{in}} \approx \left(1+\frac{R_1}{R_2}\right)\left(1-\frac{R_1+R_2}{R_2}\frac{1}{A_1}\right)$

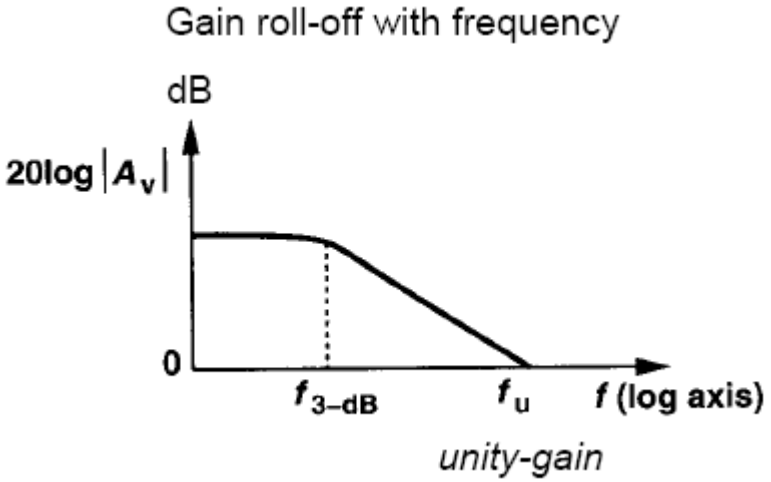
$A_1 > 1000$.

- Simple CS stage – an open-loop implementation:
  - ✓ Error 1% 미만 만들기 어렵다.
  - ✓ 왜? → NMOS, 저항 variation → ~20%

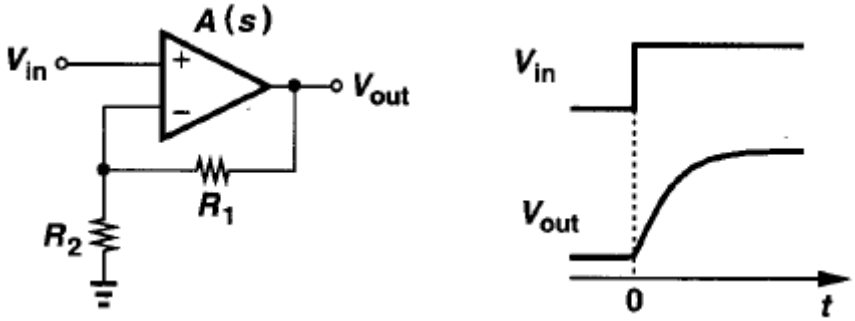


$$\left|\frac{V_{out}}{V_{in}}\right| = g_m R_D = 10$$

❑ Small-signal bandwidth



❑ Large-signal bandwidth – slew rate



Output swing

- ✓ 대부분의 시스템에서는 output swing 전압이 큰 Op-Amp를 필요로한다.

Linearity

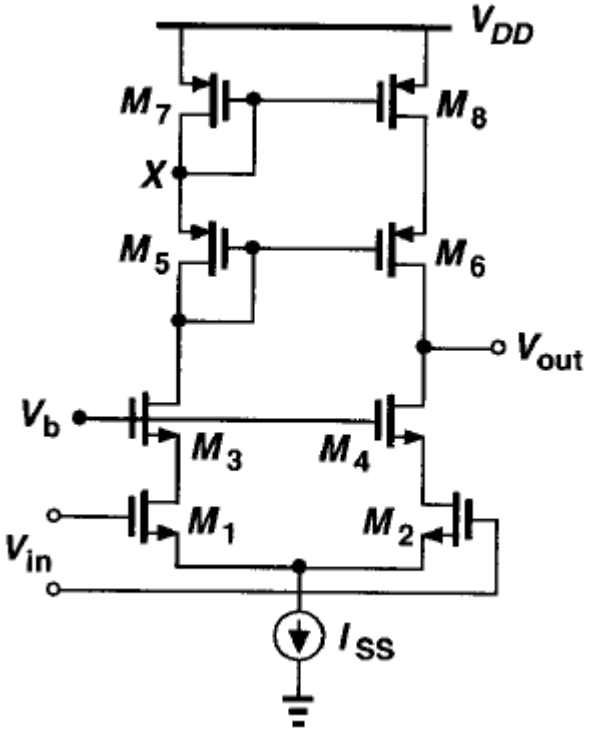
- ✓ Open-loop op amp 는 non-linearity 영향을 크게 받는다.
- ✓ input pair *M*1- *M*2 에서 입력 전압과 drain 전류 사이에 non-linearity 가 발생한다.

Noise and offset

- ✓ 입력 노이즈와 offset에 의하여 입력 전압의 최소 전압 수준이 결정된다.

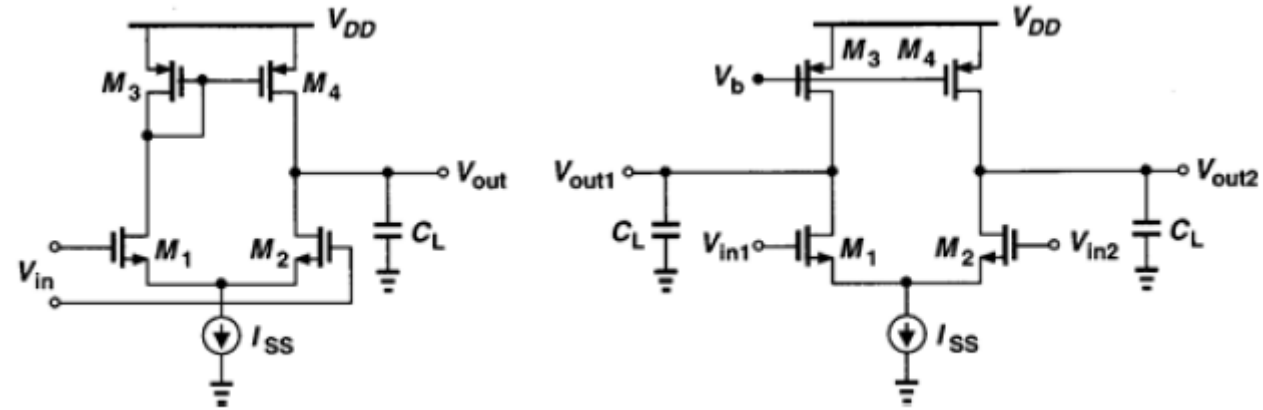
Supply rejection

- ✓ Digital 전원과 함께 사용하는 전원에 의한 노이즈를 받게 되는데, Op-amp의 성능에서 전원 노이즈를 제거하는 것이 꼭 필요하고, 따라서, differential 회로가 많이 사용된다.



9.2 One-stage op amps

- Simple op amp



Differential input & *single-ended* output

Differential input & *differential* output

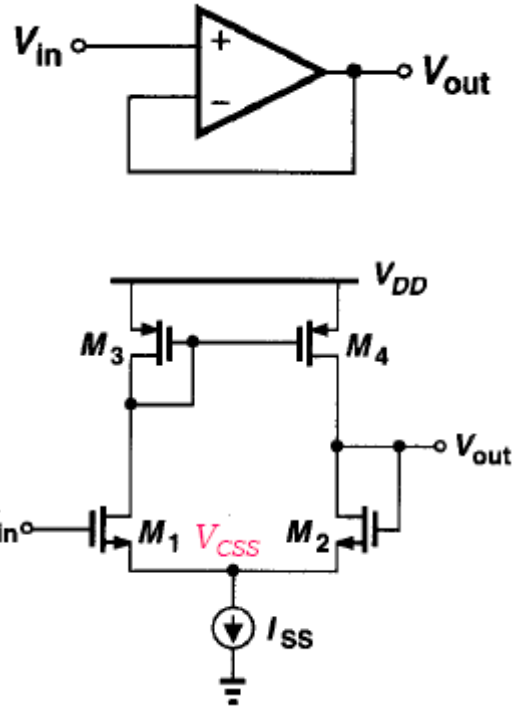
- ✓ Low frequency gain = *gmN* (*roN* || *roP*). → submicron devices 에서 20 넘기 힘들다.
- ✓ bandwidth 는C_L에 의하여 결정된다.
- ✓ *M*1-*M*4 에 의한 노이즈 영향을 받는다.

❑ Unit-gain buffer

✓ Input common-mode voltage range

$$V_{in,min} = V_{CSS} + V_{GS1}$$
$$V_{in,max} = V_{DD} - |V_{GS3}| + V_{TH1}$$

- If V_{TH}=0.7V and V_{ov}=V_{GS}-V_{TH}=0.3V,
- then $V_{in,min}$ = 1.3V and $V_{in,max}$ = 2.7V
- Input CM range = 1.4V with V_{DD}=3V



✓ Output impedance

$$R_{out} = \frac{R_{out,open}}{1+\beta A_{v,open}} = \frac{r_{oP}\|r_{oN}}{1+g_{mN}(r_{oP}\|r_{oN})} \approx \frac{1}{g_{mN}}$$

❑ Cascode op amps

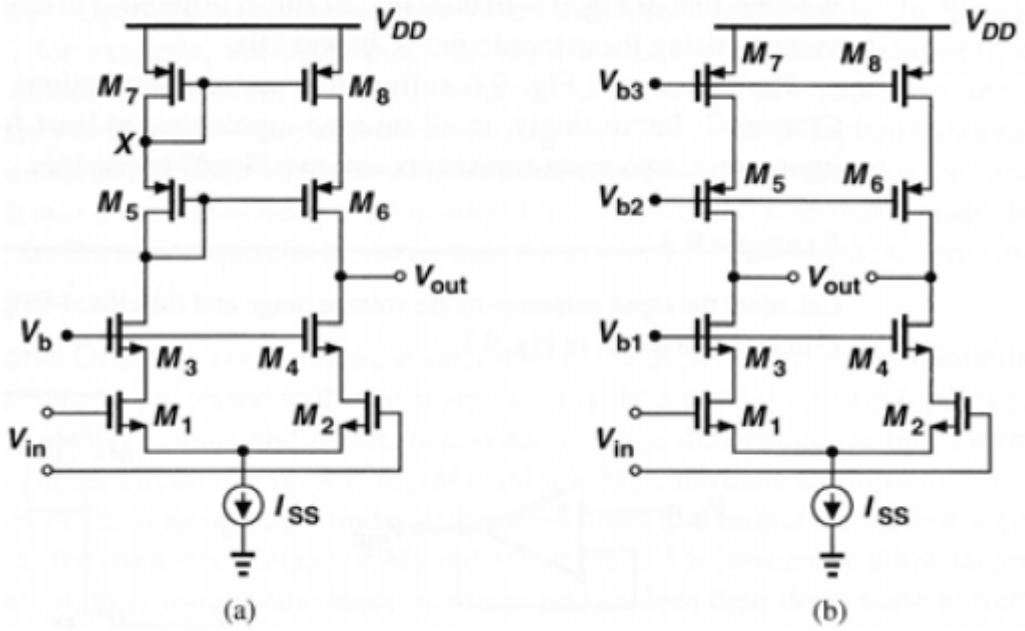
- ✓ 높은 gain을 위해서 differential cascode 사용
- ✓ Low-frequency gain

$$A_v = g_{mN}[(g_{mN} r_{oN}^2) \parallel (g_{mP} r_{oP}^2)]$$

- ✓ Output swing이 줄어듦

$$2[V_{DD} - (V_{OD1} + V_{OD3} + V_{CSS} + |V_{OD5}| + |V_{OD7}|)]$$

- ✓ pole 추가됨 → stability issue



❑ Design of fully differential telescope op amp

- ✓ V_{DD} = 3V, differential output swing = 3V, power dissipation = 10mW, voltage gain = 2000.

  $\mu_n C_{ox}$ = 60 μA/V², $\mu_p C_{ox}$ = 30 μA/V², λ_n = 0.1V⁻¹, λ_p = 0.2V⁻¹

  γ = 0, V_{THN} = $|V_{THP}|$ = 0.7V

- ✓ Power budget: V_{DD}=3V → I=3.33mA

  I_{M9} = 3mA, I_{Mb1} + I_{Mb2} = 330μA

- ✓ Output swing:

  Node X(Y) swing = 1.5V, M_3-M_6 in saturation.

  For M_9,

  $|V_{OD7}| + |V_{OD5}| + V_{OD3} + V_{OD1} + V_{OD9}$ = 1.5V

  Since $M9$ carrying largest current,

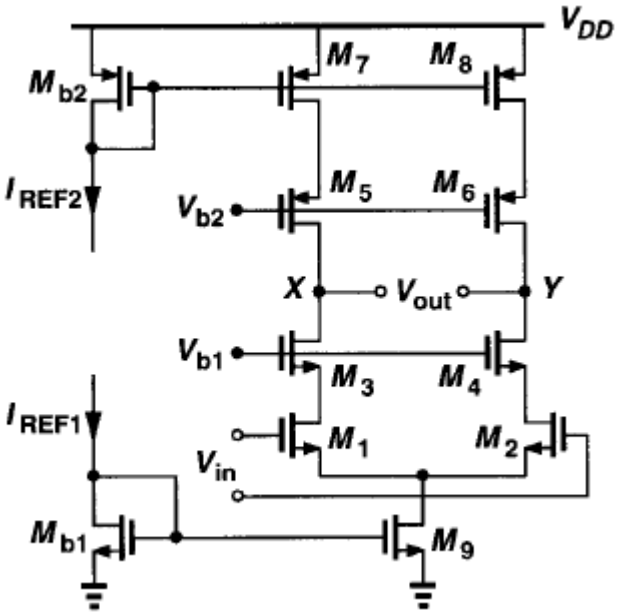
  $V_{OD9} \approx$ 0.5V is chosen. $|V_{OD5}| = |V_{OD7}| \approx$ 0.3V,

  $V_{OD1} = V_{OD3} \approx$ 0.2V.

- ✓ W/L :

  By $I_D = (1/2)\mu Cox(W/L)(V_{GS} - V_{TH})^2$, we have

  $(W/L)_{1-4}$ = 1250, $(W/L)_{5-8}$ = 1111, $(W/L)_9$ = 400.



❑ Design of fully differential telescope op amp (continue)

✓ Gain:

$A_v \approx gm1[(g_{m3}r_{o3}r_{o1}) \| (g_{m5}r_{o5}r_{o7})]$. In order to Increase the gain,

we recognize $g_m r_o = \sqrt{2\mu C_{ox}(W/L)I_D}/(\lambda I_D) \propto \sqrt{WL/I_D}$

where $\lambda \propto 1/L$. We can therefore increase the width or length.

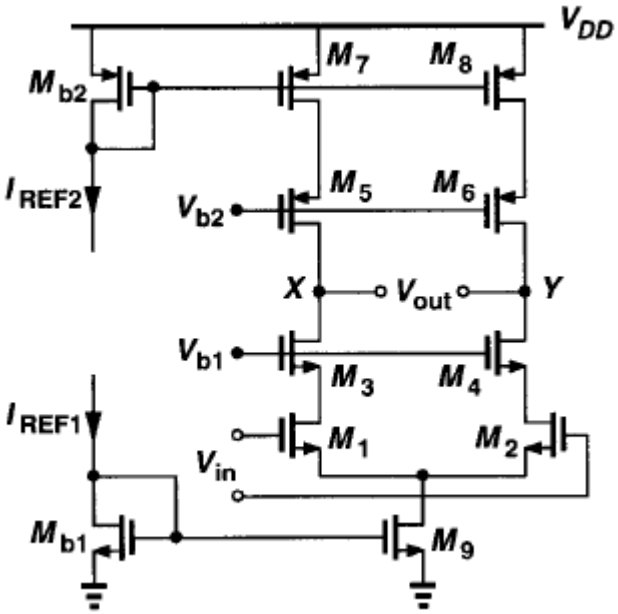
Choose $(W/L)_{5-8} = 1111\mu m/1\mu m$,
then $A_v \approx 4000$

✓ CM level & bias:

Min. allowable input CM level
$= V_{GS1} + V_{OD9} = 1.4V.$

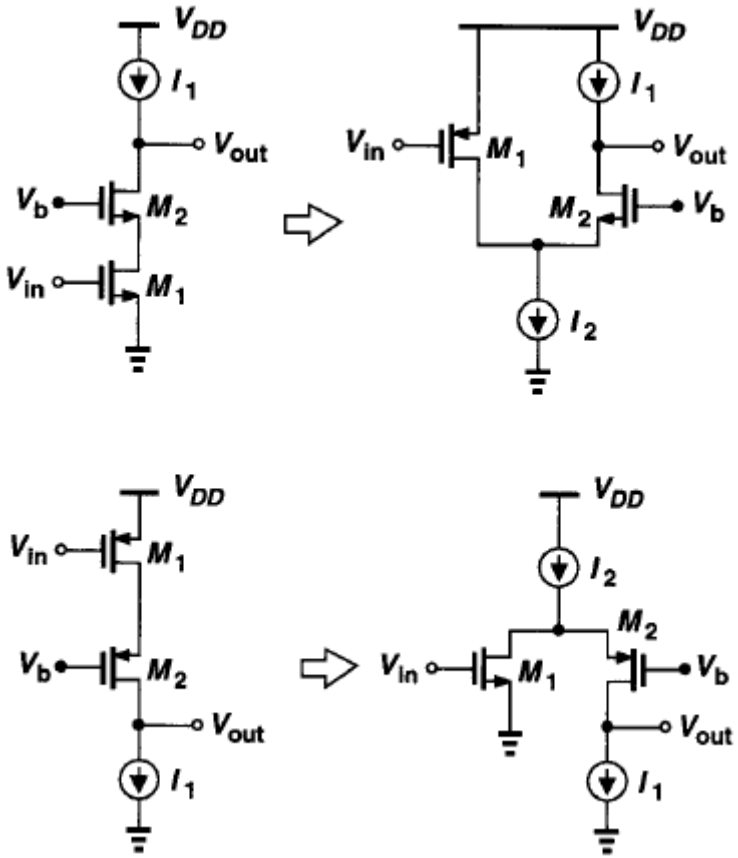
$V_{b1,\,min} = V_{GS3} + V_{OD1} + V_{OD9} = 1.6V.$

$V_{b2,\,max} = V_{DD} - (|V_{GS5}| + |V_{OD7}|) = 1.7V.$

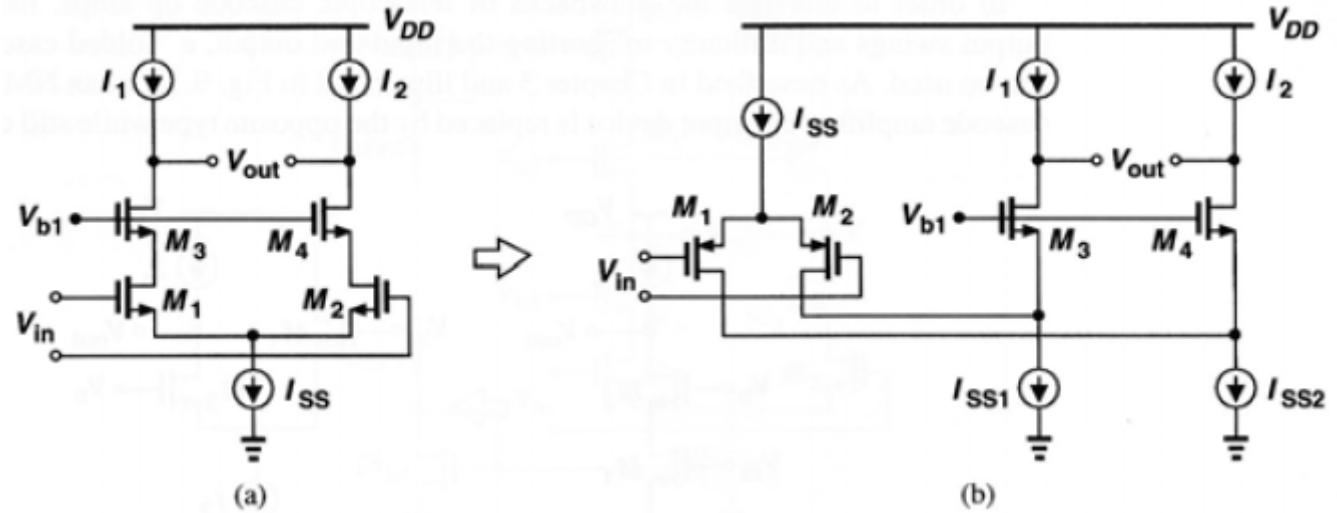


❑ Folded cascode op amps

- ✓ telescopic cascode op amp의 단점인 제한된 output swing, input과 output을 연결하기 어려운 것 등을 Folded cascode op amp는 제거할 수 있다.



❑ Folded cascode op amps (continue)

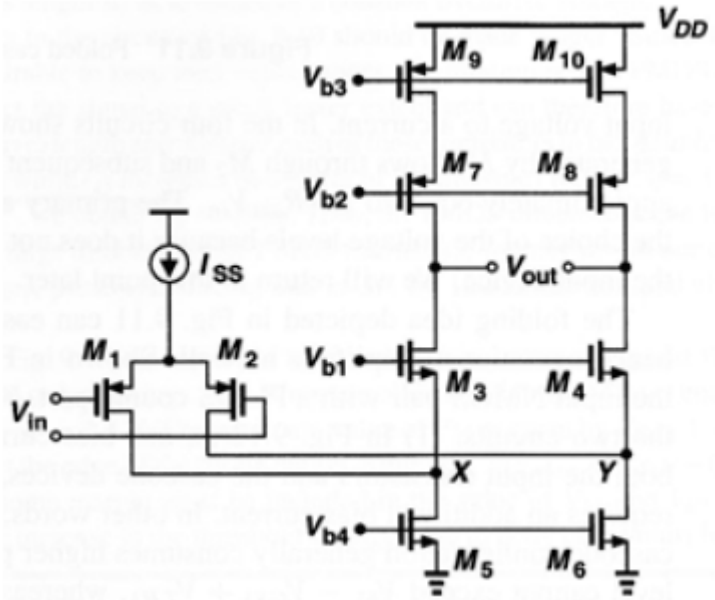


✓ 두 회로의 차이

In Fig.(a), one bias current, I_{SS}, provides the drain current of both the input transistors and the cascode devices.
In Fig.(b), the input pair requires an additional bias current, $I_{SS1} = I_{SS}/2 + I_{D3}$.

In Fig.(a), the input CM level cannot exceed $V_{b1} - V_{GS3} + V_{TH1}$,whereas in Fig.(b), it cannot be *less* than $V_{b1} - V_{GS3} + |V_{TH1}|$.

❑ Folded cascode op amps (continue)



✓ Max. output voltage swing:

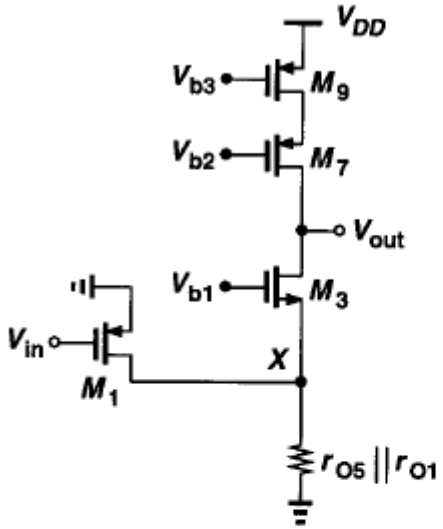
Peak-peak swing = $[V_{DD} - (|V_{OD7}| + |V_{OD9}|)] - (V_{OD3} + V_{OD5})$ for one side.

✓ Swing이 telescopic Cascode 보다 커진다.

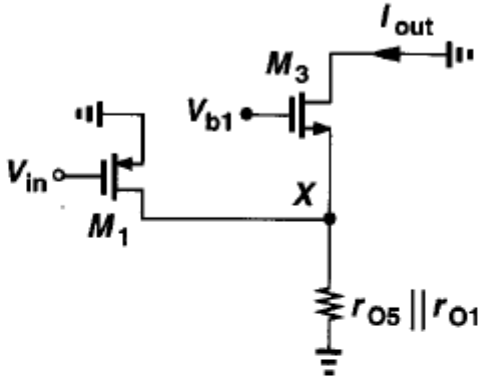
✓ *M5*와 *M6* 는 nodes *X*와 *Y* 의 cap 영향을 줄이기 위해서는 overdrive voltage를 사용해야 한다.

❑ Folded cascode op amps (continue)

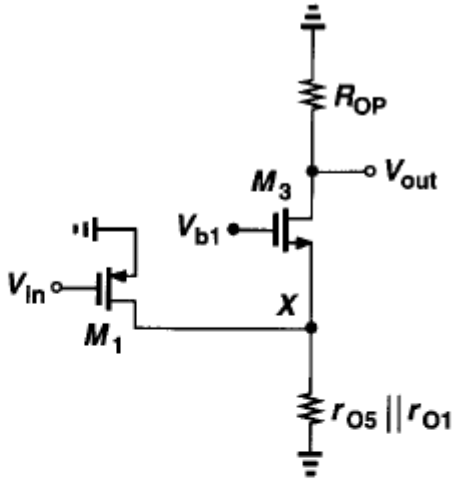
Small-signal voltage gain



Half circuit



Equivalent circuit with output shorted to ground



Equivalent circuit with output open

$|A_v| = G_m R_{out}$

Since $(g_{m3}+g_{mb3})^{-1} \| r_{o3} << r_{o1} \| r_{o5}$,

$I_{out} \approx I_{D1}$. That is $G_m \approx g_{m1}$.

$R_{OP} \approx (g_{m7} + g_{mb7})\, r_{o7}\, r_{o9}$

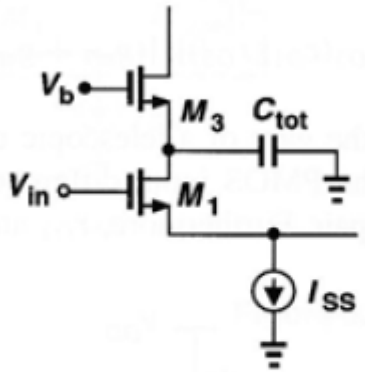
$R_{out} \approx R_{OP} \| [(g_{m3}+g_{mb3}) r_{o3} (r_{o1} \| r_{o5})]$

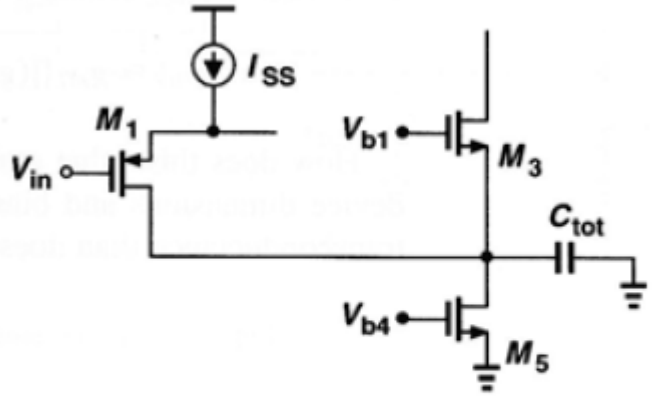
Thus, $|A_v| \approx g_{m1}\{[(g_{m3}+g_{mb3}) r_{o3} (r_{o1} \| r_{o5})] \| [(g_{m7} + g_{mb7})\, r_{o7}\, r_{o9}]\}$

The gain is usually two or three times lower than of a comparable telescopic cascode.

❑ Folded cascode op amps (continue)

Effect of device capacitance on the nondominant pole in telescopic and folded cascode op amps



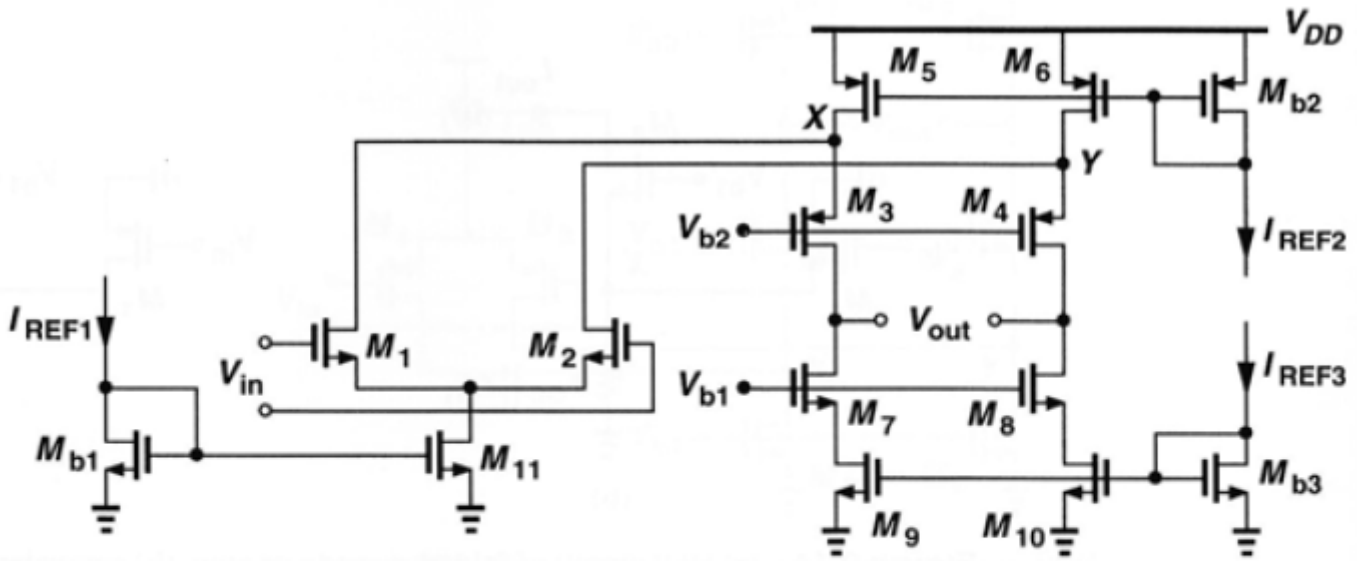


$$C_{tot} = C_{GS3} + C_{SB3} + C_{DB1} + C_{GD1}$$

$$C_{tot} = C_{GS3} + C_{SB3} + C_{DB1} + C_{GD1} + C_{GD5} + C_{DB5}$$

The pole at the "folding point," i.e., the sources of M_3 and M_4, is quite closer to the origin than that associated with the source of cascode devices in a telescopic topology.

❑ A high-gain folded cascode op amp

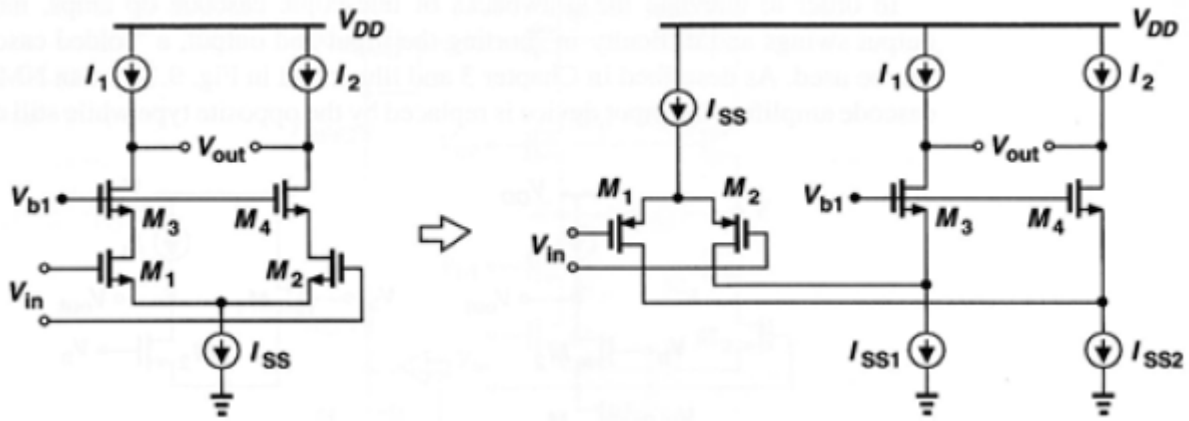


The circuit provides a higher gain because of the greater mobility of NMOS devices, but at the cost of lowering the pole at the folding point,

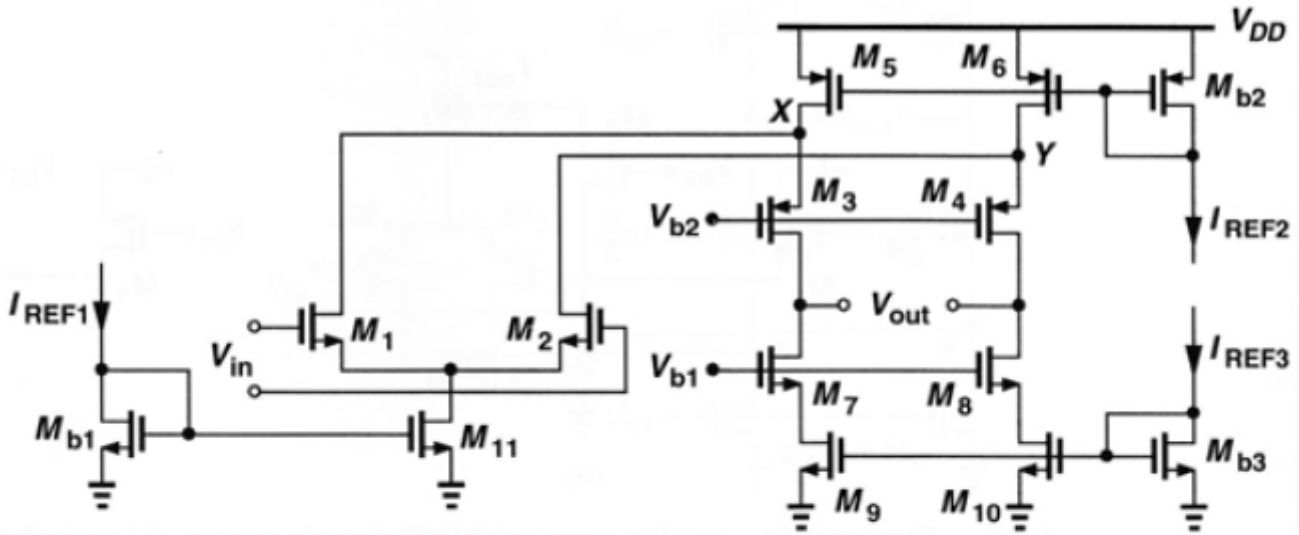
$$\omega_{p,X} \approx (g_{m3} + g_{mb3}) \;/\; C_{tot,X}.$$

❑ Telescopic- vs. folded-cascode op amps: Discussion

- ✓ folded-cascode op amp가 Telescopic-cascode op amp 보다 swing 범위가 크다는 장점을 제외하는 많은 단점을 가진다.
- ✓ 단점: higher power dissipation, lower voltage gain, lower pole frequencies, and higher noise.
- ✓ Folded-cascode op amp 가 많이 사용되는 이유는input common-mode level을 쉽게 조절 가능하기 때문이다.



❑ Design of folded-cascode op amp



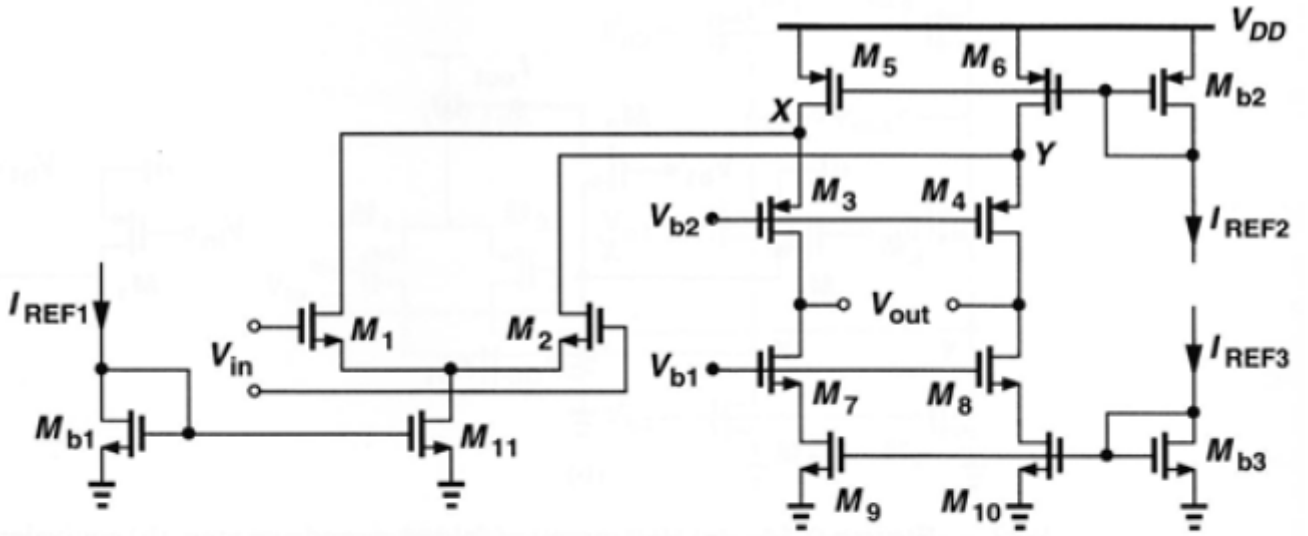
Specifications:

V_{DD} = 3V, differential output swing = 3V,

power dissipation = 10mW, voltage gain = 2000.

Assume $\mu_n C_{ox}$ = 60 μA/V², $\mu_p C_{ox}$ = 30 μA/V², λ_n = 0.1V⁻¹, λ_p = 0.2V⁻¹ (for an effective channel length of 0.5 μm), γ = 0, $V_{THN} = |V_{THP}|$ = 0.7V.

❑ Design of folded-cascode op amp (continue)



Power budget: I_{M11} = 1.5mA, I_{M9} + I_{M10} = 1.5mA, I_{Mb1} + I_{Mb2} + I_{Mb3} = 330μA.

Output swing: one side o/p swing = 1.5V, M_3-M_{10} in saturation.

Choose $|V_{OD5,6}| \approx 0.5\text{V}$, $|V_{OD3,4}| \approx 0.4\text{V}$, $V_{OD7,8} = V_{OD9,10} \approx 0.3\text{V}$.

W/L : By $I_D = (1/2)\mu Cox(W/L)(V_{GS} - V_{TH})^2$, we have

$(W/L)_{5,6} = 400$, $(W/L)_{3,4} = 313$, $(W/L)_{7-10} = 555$.

O/p CM level: CM_{min} = 0.6V, CM_{max} = 2.1V, thus CM_{opt} = 1.35V.

❑ Design of folded-cascode op amp (continue)

Determine $(W/L)_{1,2}$: min. input CM level = $V_{GS1} + V_{OD11}$.

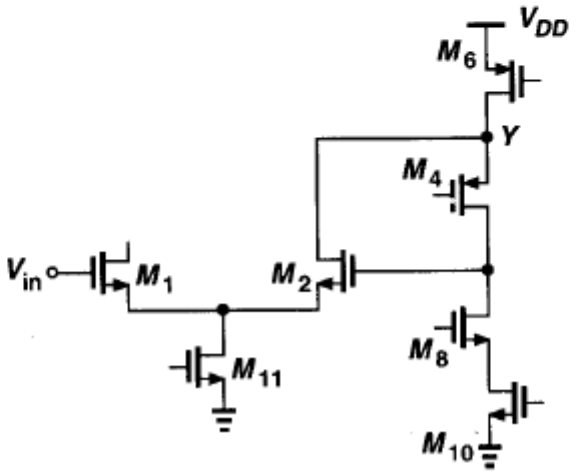
If input and output are shorted, then $V_{GS2} + V_{OD11} = 1.35\text{V}$,
and $V_{GS1} = 0.95\text{V} \Rightarrow V_{OD1,2} = 0.25\text{V} \Rightarrow (W/L)_{1,2} = 400$.
The maximum dimensions of $M_{1,2}$ are determined by the tolerable input capacitance at nodes *X* and *Y*.

Gain: $g_m = 2I_D/(V_{GS} - V_{TH})$, we have

$g_{m1,2} = 0.006\ \text{A/V}$, $g_{m3,4} = 0.0038\ \text{A/V}$, $g_{m7,8} = 0.05\ \text{A/V}$.

For $L = \text{x}\ \mu\text{m}$, find r_o.

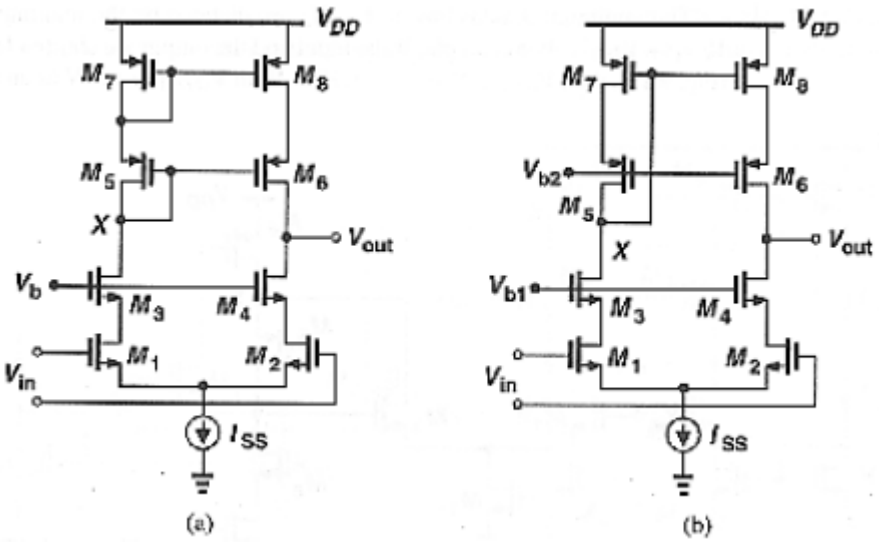
Note $|A_v| \approx g_{m1}\{[(g_{m3} + g_{mb3})r_{o3}(r_{o1} \parallel r_{o5})] \parallel [(g_{m7} + g_{mb7})\ r_{o7}r_{o9}]\}$



❑ Cascode op amps with single-ended output

Fig(a): $V_X = V_{DD} - |V_{GS5}| - |V_{GS7}|$, limiting the maximum value of V_{out} to $V_{DD} - |V_{GS5}| - |V_{GS7}| - |V_{TH6}|$ and wasting one PMOS threshold voltage in the swing.

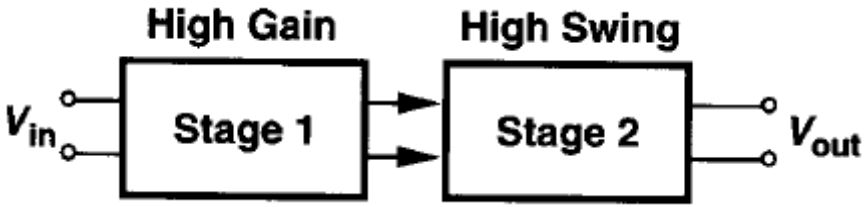
Fig(b): To solve above issue, M_7 and M_8 are biased at the edge of the triode region.



- swing 전압이 반으로 줄어든다.
- Node X에 pole을 가진다. → feedback speed를 제한한다.

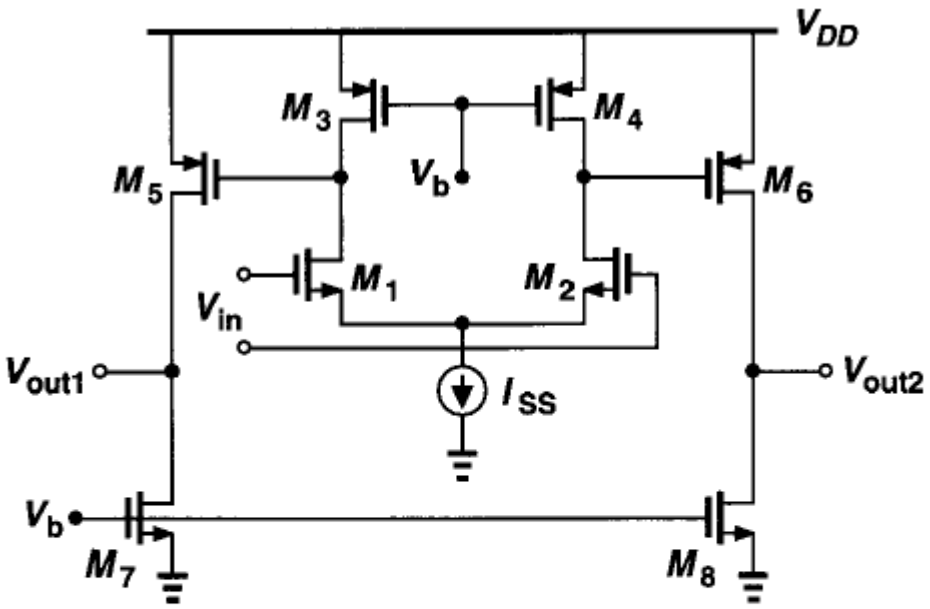
✓ Differential 이 많이 사용된다.

9.3 Two-stage op amps



- Two-stage op amp의 특징
  - ✓ One stage op amp의 gain = g_m x R_{out} → gain ↑ → Cascoding → output swing ↓
  - ✓ Output swing 을 크게 하면서 gain을 얻으려면 → Two-stage op amp→ pole 수 증가 → feedback 시스템에서 stability 문제 발생
  - ✓ Two-stage op amp 구성 = stage #1 (high gain) + stage #2 (high swing)

❑ Simple implementation of a two-stage op amp



Gain:

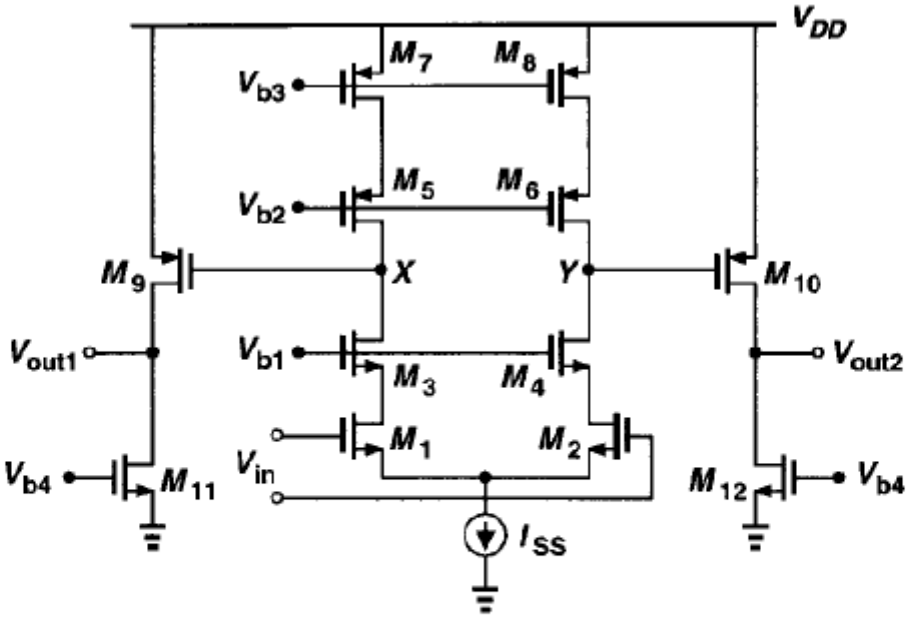
$$A_{v,\text{1st stage}} = g_{m1,2}(r_{o1,2} \parallel r_{o3,4})$$

$$A_{v,\text{2nd stage}} = g_{m5,6}(r_{o5,6} \parallel r_{o7,8})$$

$$\text{Overall gain } A_v = A_{v,\text{1st stage}} \times A_{v,\text{2nd stage}}$$

$$\text{Output swing} = V_{DD} - |V_{OD5,6}| - V_{OD7,8}$$

❑ Two-stage op amp employing cascoding

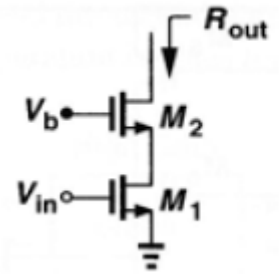


To obtain a higher, the first stage incorporate cascode devices. The overall voltage gain is

$$A_v \approx \{g_{m1,2}[(g_{m3,4} + g_{mb3,4})r_{o3,4}r_{o1,2}] \parallel (g_{m5,6} + g_{mb5,6})r_{o5,6}r_{o7,8}]\} \times [g_{m9,10}(r_{o9,10} \parallel r_{o11,12})]$$

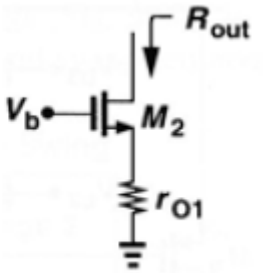
9.4 Gain boosting

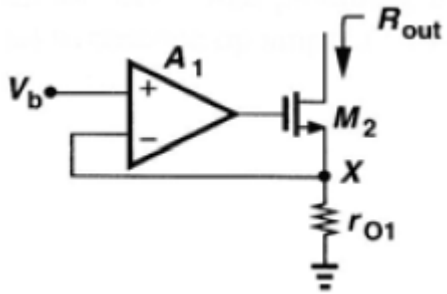
- Gain boosting
  - ✓ Gain을 높이는 것은 출력 저항을 높이는 것이다.
  - ✓ Gain boosting 은 Cascode를 사용하지 않고 출력 저항을 높여준다.



$R_{out} = g_{m2} r_{o2} r_{o1}$

M_1 operates as a degeneration resistor.



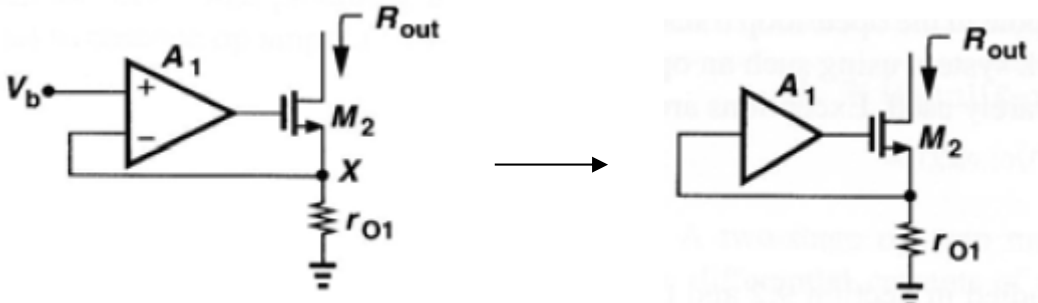


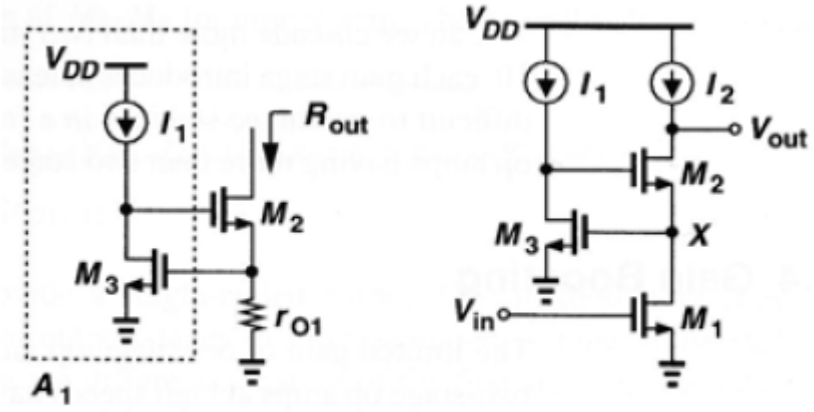
$R_{out} \approx A_1 g_{m2} r_{o2} r_{o1}$

❑ Gain boosting 증명

❑ Gain boosting in cascode stage

✓ 소신호 동작에서 , V_b=0





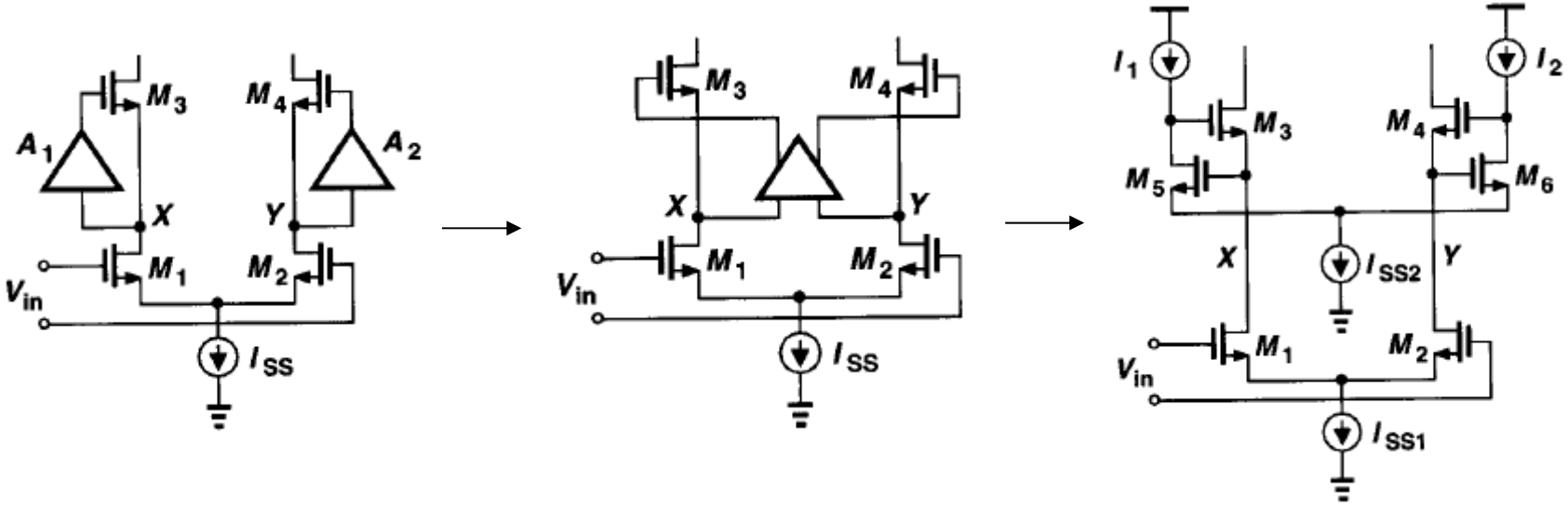
regulated cascode

$$|A_v| \approx g_{m1}\,(g_{m2}\,r_{o2}\,r_{o1})\,(g_{m3}\,r_{o3})$$

$V_X = V_{GS3}$이므로,

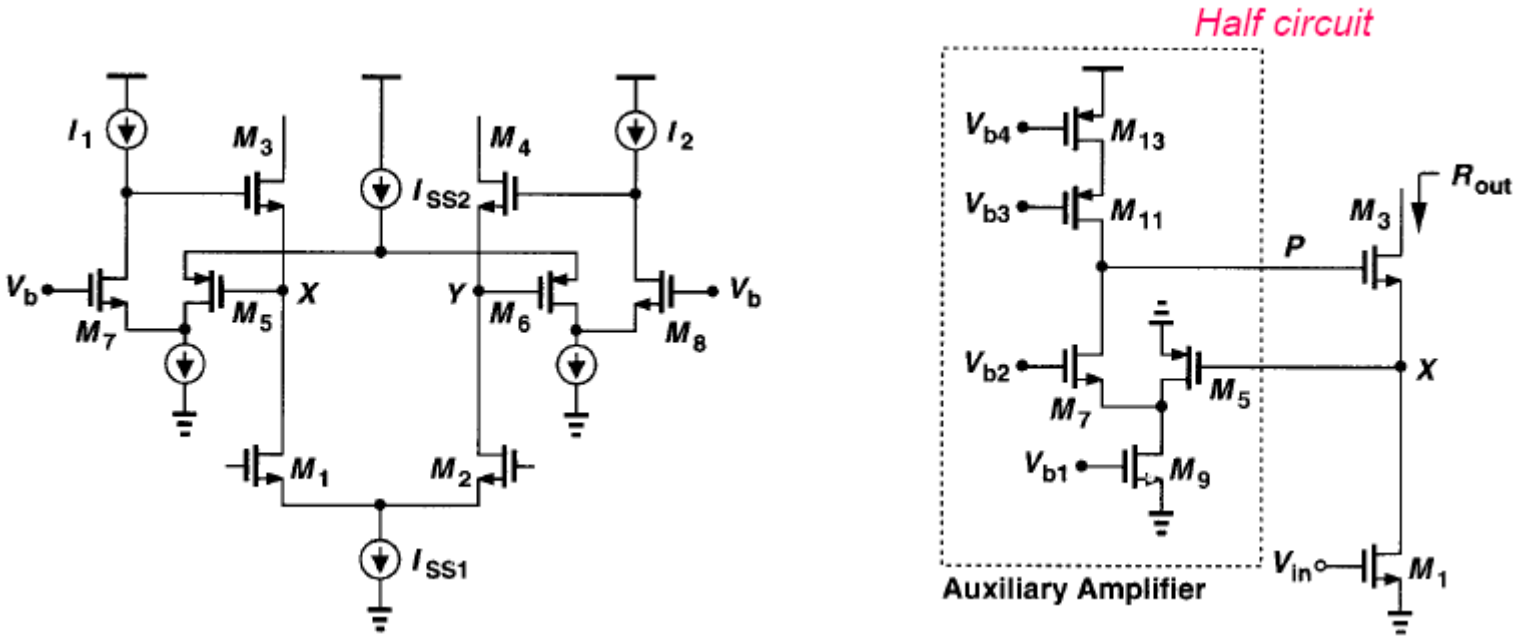
$V_{out} \geq V_{OD2} + V_{GS3}$.

❑ Boosting output impedance of a differential cascode stage



$V_X = V_{GS5} + V_{ISS2}$이므로, $V_{out} \geq V_{OD3} + V_{GS5} + V_{ISS2}$

❑ Folded-cascode circuit used as auxiliary amplifier



If nodes X and Y are sensed by a PMOS pair, the minimum value of V_X and V_Y is not dictated by the gain-boosting amplifier.

The minimum allowable level of V_X and V_Y is given by $V_{OD1,2} + V_{ISS1}$.

Output impedance: Since $\dfrac{V_P}{V_X} = g_{m5}R_{out1}$

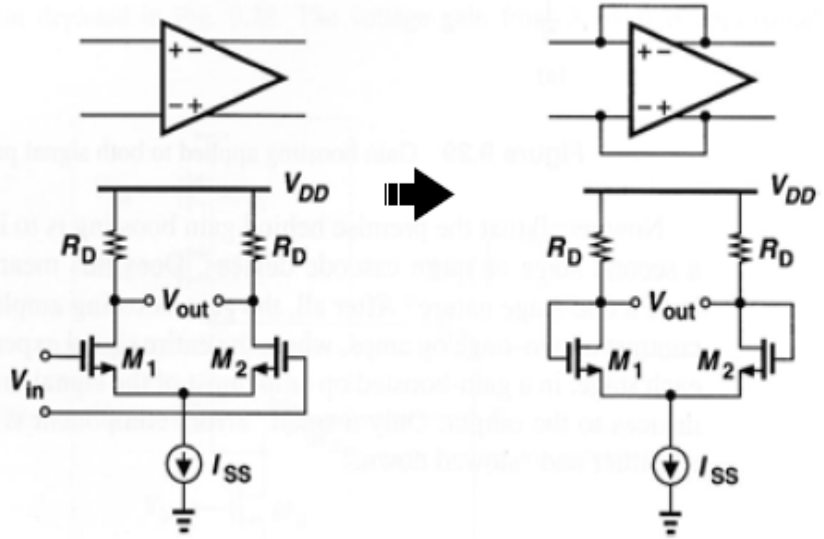
where $R_{out1} \approx [g_{m7}r_{o7}(r_{o9}\|r_{o5})] \parallel (g_{m11}r_{o11}r_{o13})$, $R_{out} \approx g_{m3}r_{o3}r_{o1}g_{m5}R_{out1}$.

9.5 Comparison of various op amps

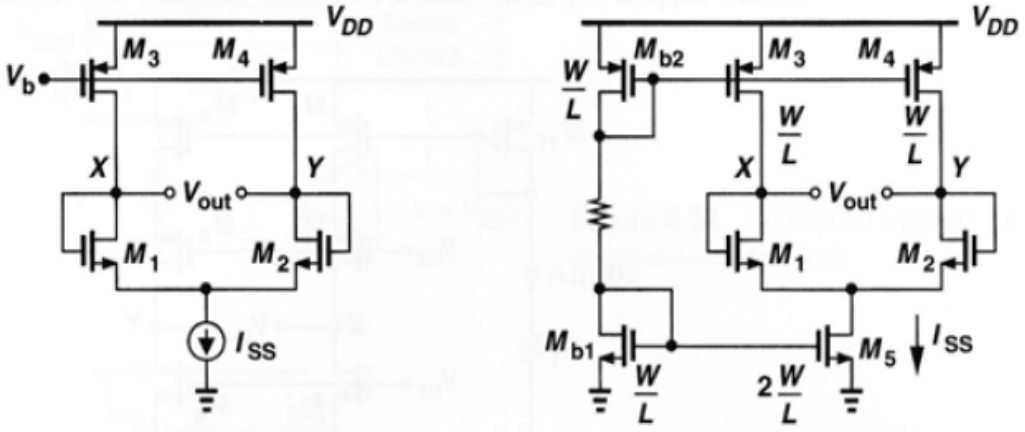
	Gain	Output Swing	Speed	Power Dissipation	Noise
Telescopic	Medium	Medium	Highest	Low	Low
Folded-Cascode	Medium	Medium	High	Medium	Medium
Two-stage	High	Highest	Low	Medium	Low
Gain-Boosted	High	Medium	Medium	High	Medium

8.6 Common-mode feedback (CMFB)

- Full differential circuits의 single-ended circuits에 대한 장점
  - ✓output swings 증가
  - ✓mirror poles 피할 수 있어서 higher closed-loop speed
- 그러나, high-gain differential circuits 은 common-mode feedback.
- Simple differential pair (입력과 출력을 short 시킴)
  - ✓Input & output common-mode level → $V_{DD} - I_{SS} R_D / 2$



❑High-gain differential pair (입력과 출력을 short 시킴)



❑nodes X and Y 에서의 common-mode level ?

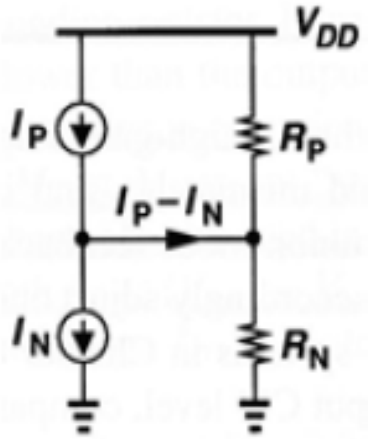
- ✓입력 TR M1, M2가 전류 I_{SS} /2 를 통과시킨다면, CM level 은 I_{D3} 와 I_{D4} 가 얼마나 같은가에 의하여 결정된다.

❑Effect of current mismatches: Mismatches in PMOS and NMOS current mirrors

- ✓current mirror→ ID5 = I_{SS} & ID3,4 = I_{SS} /2.
- ✓If $I_{D3,4} > I_{SS}$ /2, → M3와 M4 는 triode region → drain currents fall to ISS /2.
- ✓If $I_{D3,4} < I_{SS}$ /2, → V_X 와V_Y 는 낮아짐 → M5는 triode region → M5의 전류 $2 \times I_{D3,4}$.

❑Simplified model of high-gain amplifier

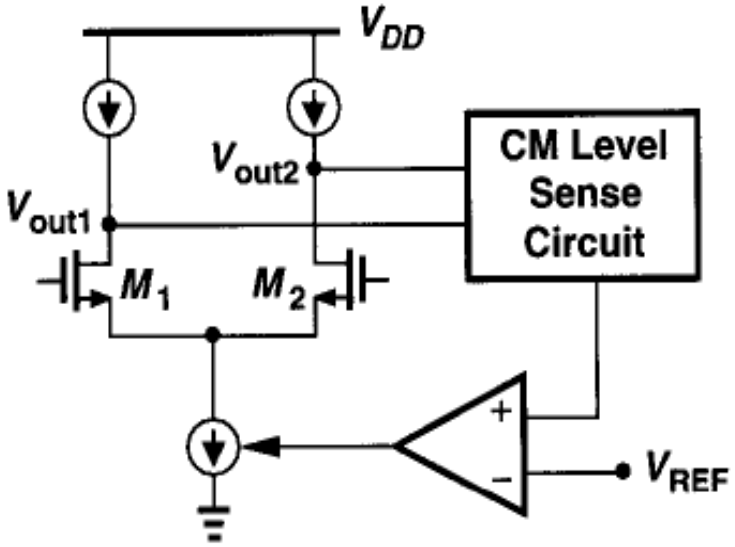
✓high-gain amplifiers에서 p-type / n-type 전류를 정확하게 맞추어야 한다.



$$\Delta V = (I_P - I_N)(R_P \| R_N)$$

✓Mismatch → current error 발생 → $R_P||R_N$ 이 큼 → voltage error 이 커짐 → p-type / n-type current source 가 triode region

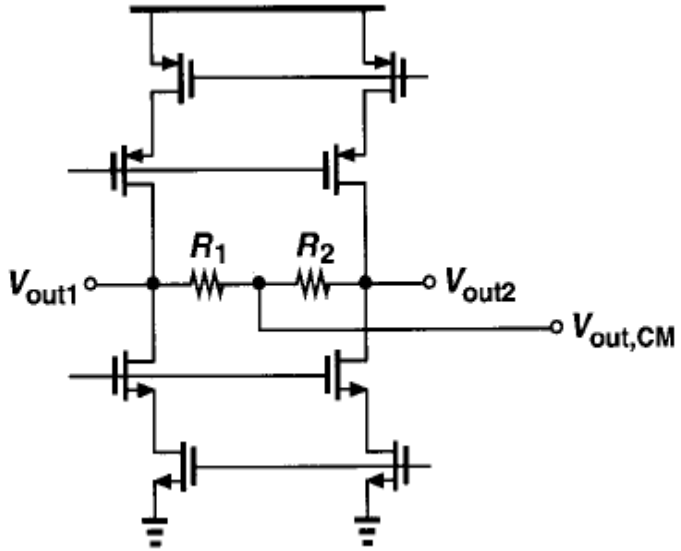
❑Conceptual topology for CMFB.



✓high-gain amplifiers 에서 output CM level 은 공정 특성과 mismatch에 민감하지만 differential feedback 으로는 안정화 시키기 어렵다.

✓CMFB network = 두 출력의 CM level을 감지 → bias current 중 하나를 조정

❑CMFB with resistive sensing



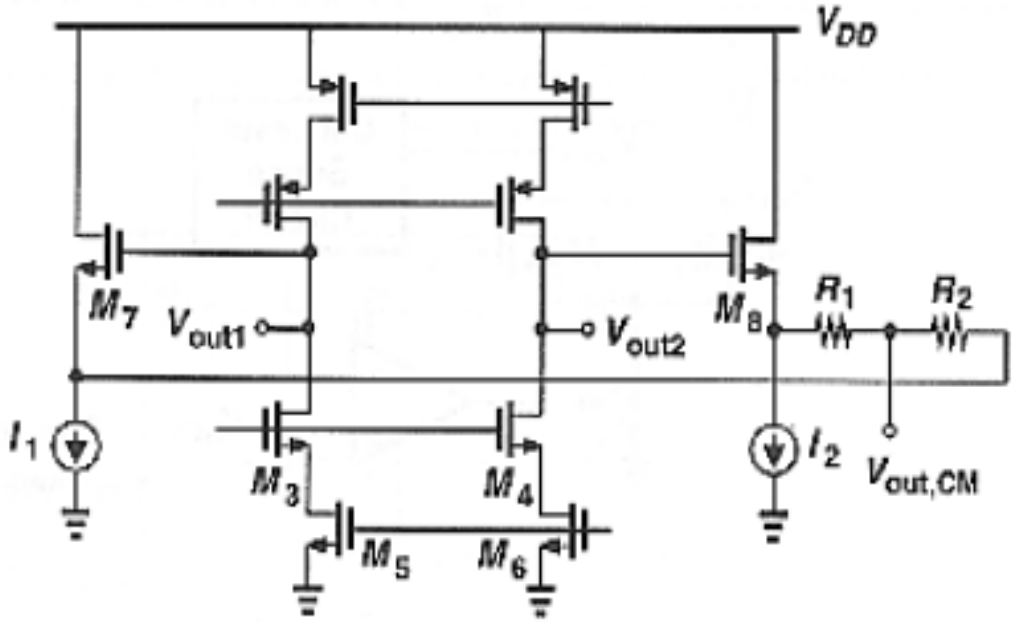
✓Output CM level → $V_{out,CM} = (V_{out1} + V_{out2})/2$

✓Resistive divider level

→ $V_{out,CM} = (R_1V_{out2} + R_2V_{out1})/(R_1 + R_2)$ → $(V_{out1} + V_{out2})/2$, if $R_1 = R_2$.

✓R_1과 R_2 는 open-loop gain에 영향을 주지 않기 위해서 출력 저항보다 커야 한다.

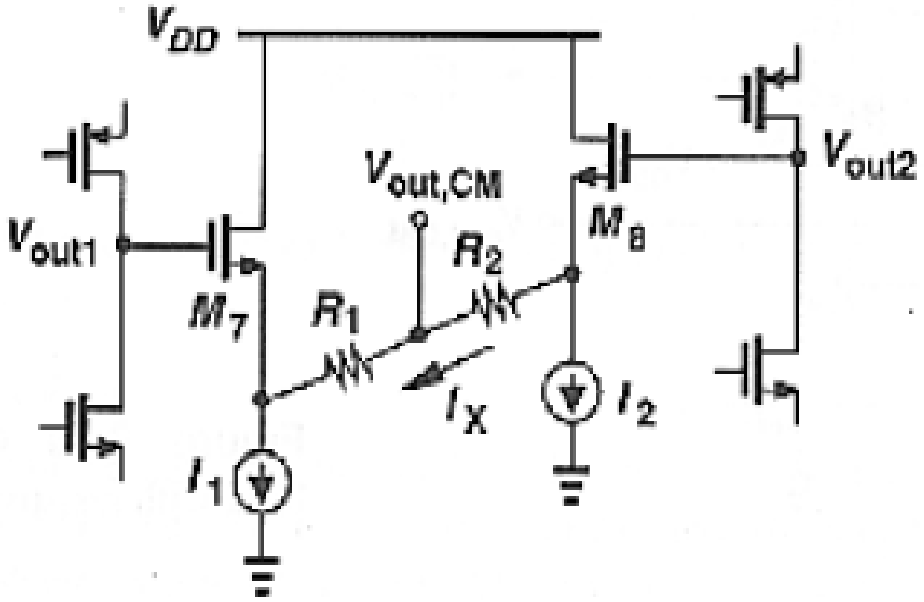
❑CMFB using source followers



❑output CM level이 $V_{GS7,8}$ 만큼 줄지만 보상에서 고려되기 때문에 상관없다.

✓R1, R2, I1, I2 큰 출력을 영향 주지 않을 만큼은 커야 한다.

❑CMFB using source followers

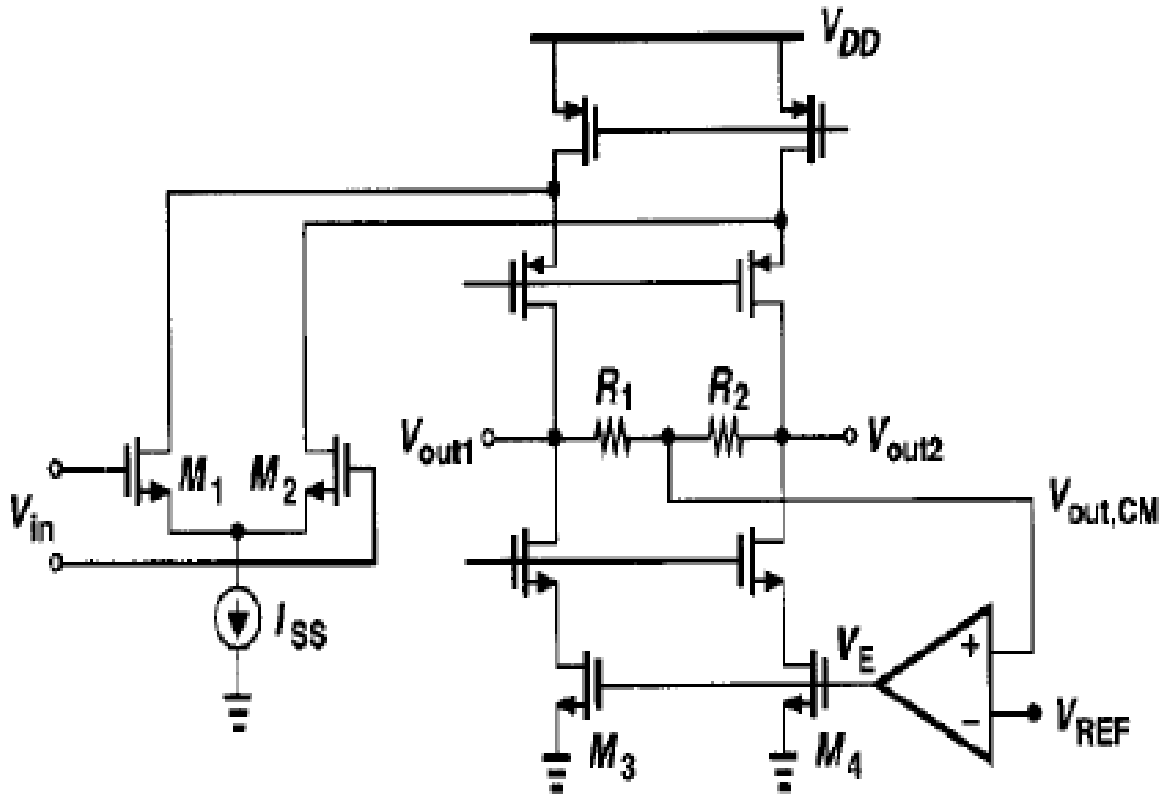


✓If $V_{out2} >> V_{out1}$, I_1에 모든 전류가 흐른다.

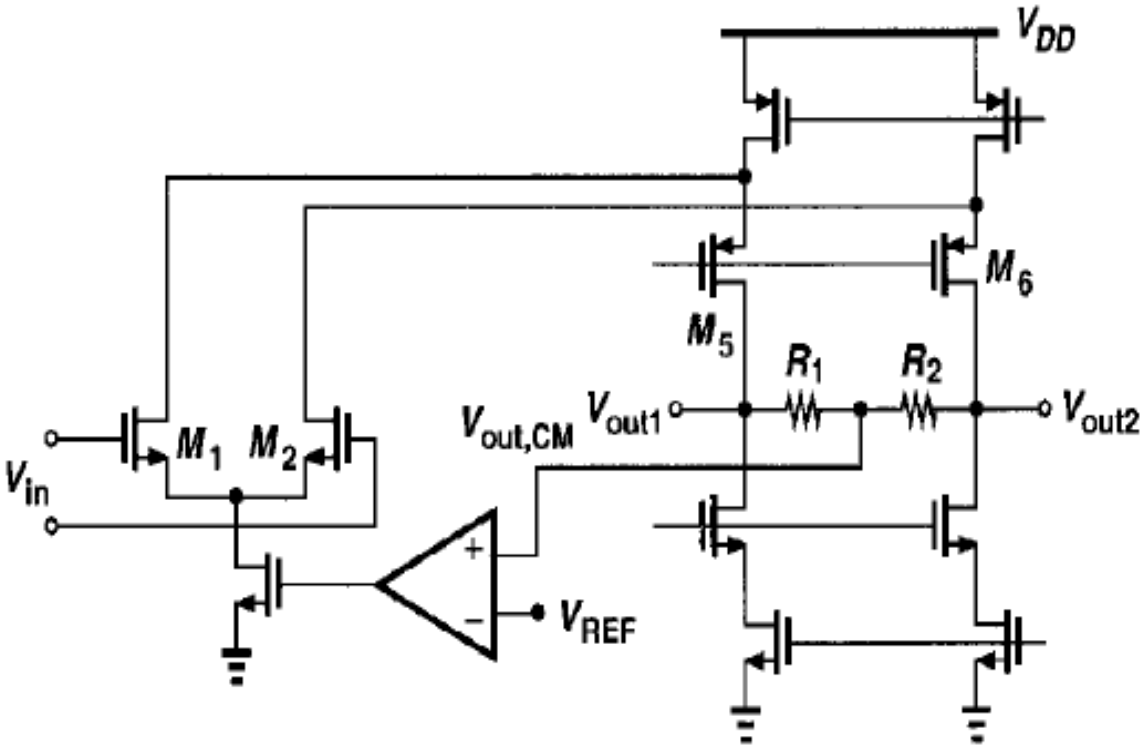
✓$IX \approx (V_{out2} - V_{out1})/(R_1 + R_2)$

✓$(R_1 + R_2)$ 또는 I_1 이 충분히 크지 못하면 → $I_{D7} \sim 0$ → $V_{out,CM}$ 이 output CM level 을 반영하지 못한다.

❑Sensing and controlling output CM level

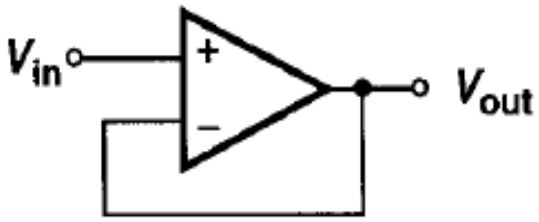


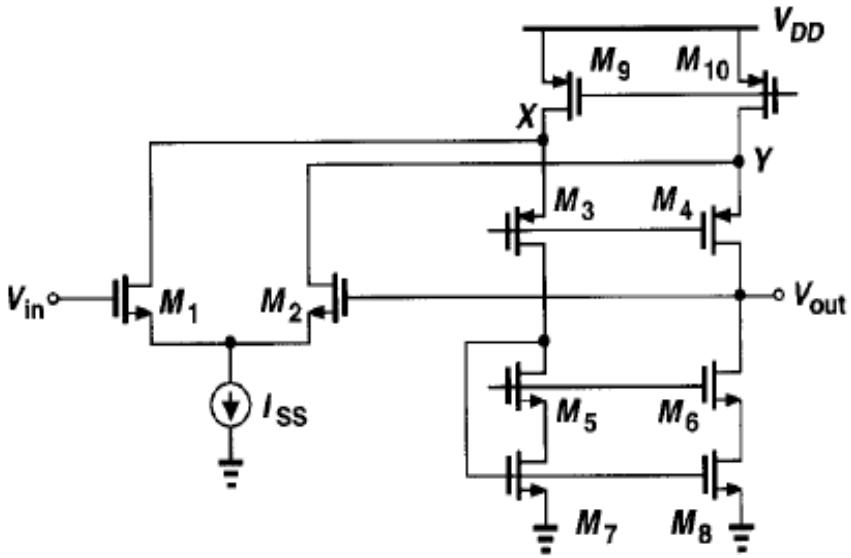
❑Alternative method of controlling output CM level



9.7 Input range limitations

❑Differential input swing은 보통 매우 작지만, unit-gain buffer의 경우 넓은 input swing 을 필요로 한다.

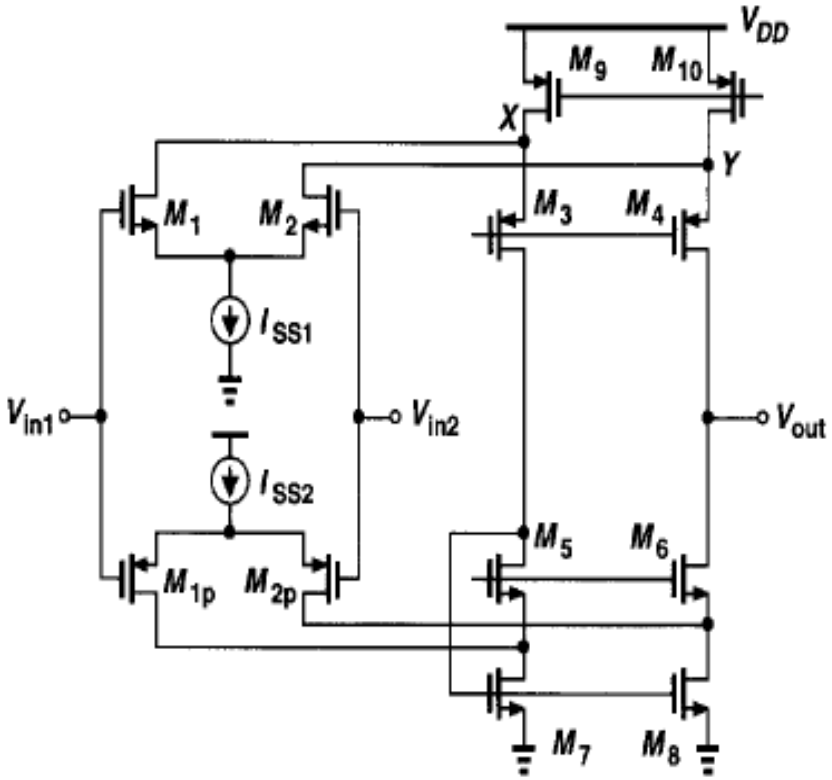




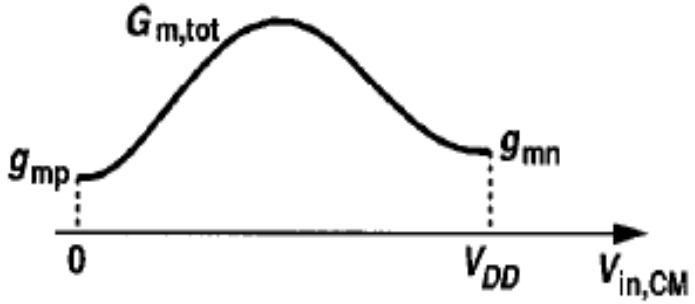
✓$V_{in,min} \approx V_{out,min} = V_{GS1,2} + V_{ISS}$.

✓If $V_{in} < V_{in,min}$ → MOS transistor (I_{SS}) enters triode region → bias current ↓→ transconductance ↓

❑Extension of input CM range

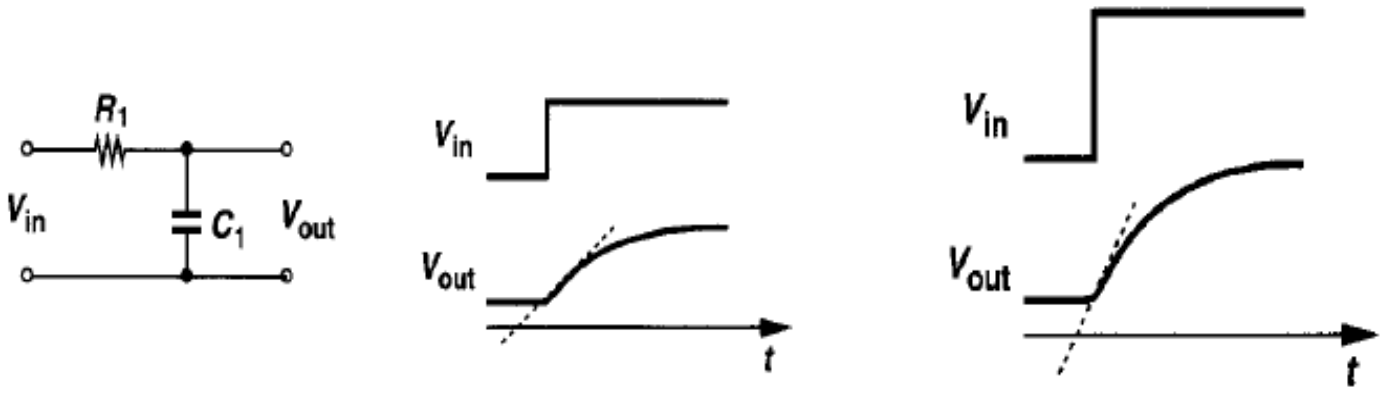


Variation of equivalent transconductance with the input CM level.



9.8 Slew rate

❑Response of a linear circuit to input step



- dV_{out}/dt: Since $V_{out} = V_0[1 - \exp(-t/\tau)]$, where $\tau = RC$, we have

$$\frac{dV_{out}}{dt} = \frac{V_0}{\tau}\exp\frac{-t}{\tau}$$

- $dV_{out}/dt \propto V_0$; if we apply a larger input step, the output rises more rapidly.

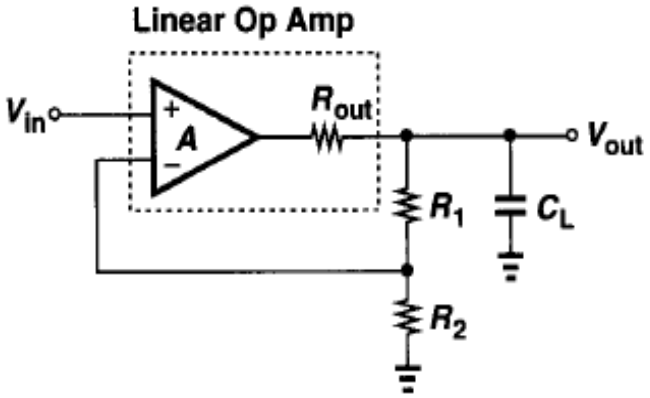
❑Response of a linear op amp to step response

- Assume op amp is linear,

$$\left[\left(V_{in}-V_{out}\frac{R_2}{R_1+R_2}\right)A-V_{out}\right]\frac{1}{R_{out}}=\frac{V_{out}}{R_1+R_2}+V_{out}C_L s$$

Assume $R_1 + R_2 >> R_{out}$, we have

$$\frac{V_{out}}{V_{in}}(s)\approx\frac{A}{\left(1+A\frac{R_2}{R_1+R_2}\right)\left[1+\frac{R_{out}C_L}{1+AR_2/(R_1+R_2)}s\right]}$$



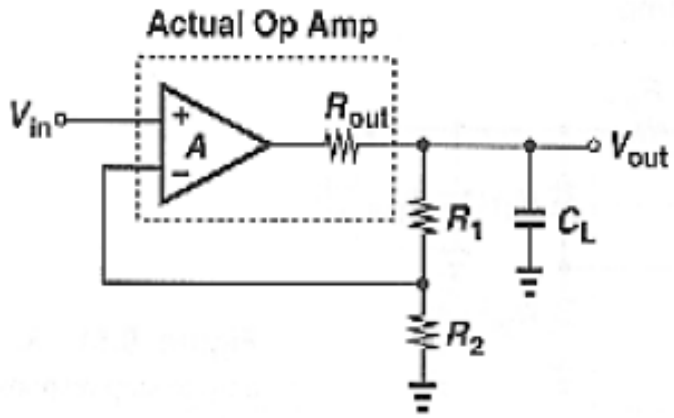
The step response is given by

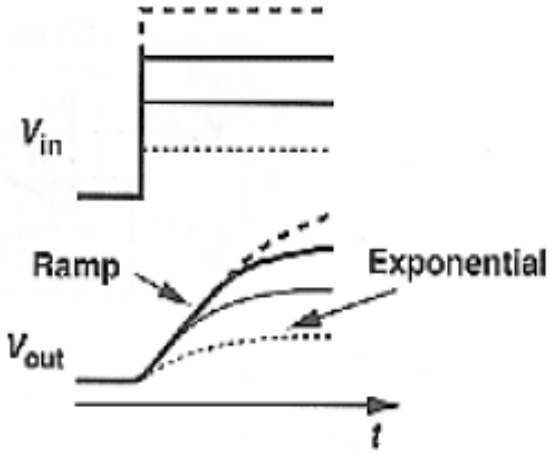
$$V_{out}=V_0\frac{A}{1+A\frac{R_2}{R_1+R_2}}\left(1-\exp\frac{-t}{\frac{C_L R_{out}}{1+AR_2/(R_1+R_2)}}\right)u(t)$$

indicating that the slope is proportional to the final value.
This type of response is called "linear settling."

❑Slewing in an op amp circuit

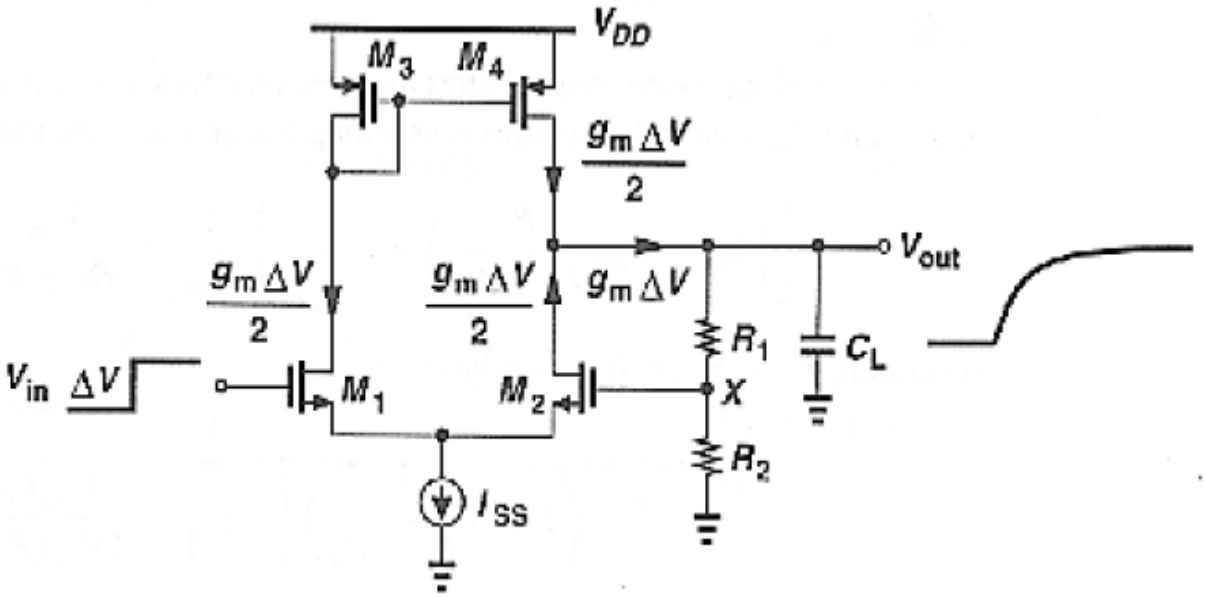
✓작은 입력 신호에는 exponential 함수로 증가하지만 큰 입력 신호에서는 선형적으로 증가한다.



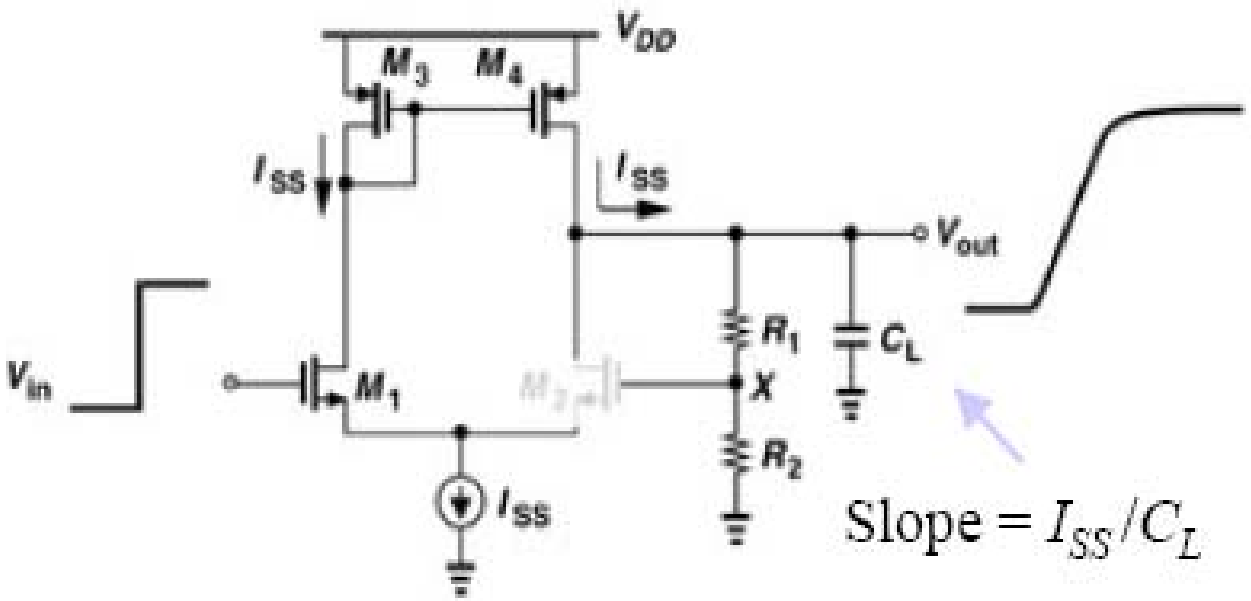


$$V_{out} = V_0 \frac{A}{1 + A\dfrac{R_2}{R_1 + R_2}} \left(1 - \exp \frac{-t}{\dfrac{C_L R_{out}}{1 + AR_2/(R_1 + R_2)}} \right) u(t) \qquad \text{.....(A)}$$

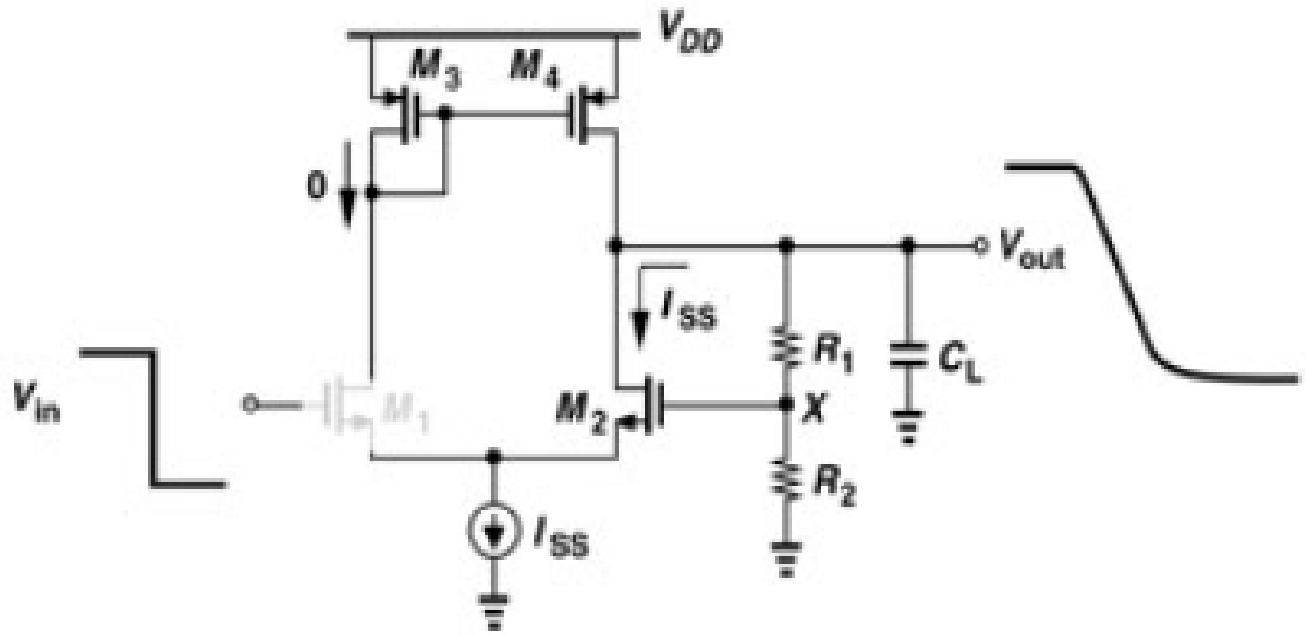
❑Small-signal operation of a simple op amp



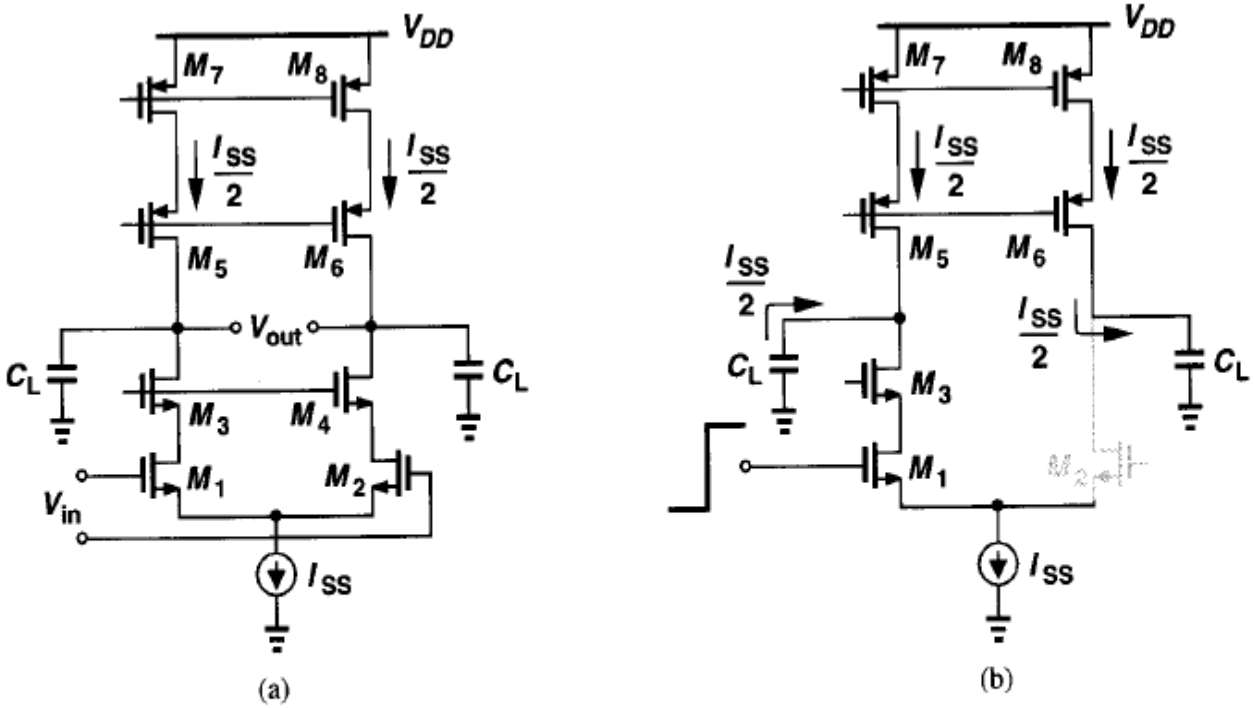
❑Small-signal operation of a simple op amp



❑Small-signal operation of a simple op amp



❑Slewing in telescopic op amp



V_{out1} and V_{out2} appear as a ramps with slopes equal to $\pm I_{SS}/(2C_L)$, and consequently $V_{out1} - V_{out2}$ exhibits a slew rate equal to I_{SS}/C_L.

❑Slewing in folded-cascode op amp

- If $I_P \geq I_{SS}$, the slew rate is equal to I_{SS}/C_L, independent of I_P.